PACKAGING TWG

Contents

Executive Summary 1
Introduction 3
Situational (Infrastructure) analysis 5
Manufacturing Equipment 5
Manufacturing Processes 6
Package/System Co-Design and Simulation 6
Heterogeneous Integration 9
Materials 10
Package Substrates 10
New Packaging Materials 11
Quality/Reliability 14
Environmental Technology 14
Test, Inspection, Measurement (TIM) 14
Roadmap of Quantified Key Attribute Needs 15
Silicon interposer 15
Organic interposer 15
Optical Packaging/Integration 17
Electrical Packaging/Integration 19
Thermo-Mechanical Packaging 20
Critical (Infrastructure) Issues 21
Wafer Level Packaging 21
Panel Processing 24
Technology Needs 26
Prioritized Research Needs (> 5 years result) 26
Prioritized Development & Implementation Needs (< 5 years result) 27
Gaps and Showstoppers 32
References 3
Contributors 3

EXECUTIVE SUMMARY

Introduction: Packaging of integrated photonic devices presents numerous technological, manufacturing and cost challenges. Historically, packaging has been accepted to be a high-cost step in the overall manufacturing process, often consuming more than 80% of the total manufacturing cost. However, as new mass markets for integrated photonics open and unit demand steadily increases, a clear roadmap for packaging of integrated photonic devices becomes more critical. This ensures that more cost-effective and volume scalable packaging processes can be implemented. In terms of this roadmap, packaging can be seen as the assembly of photonic and electronic devices from chip to board, encompassing optical fibers, micro optics, electronic IC packaging using wirebonding, flipchip assembly, thermal management and mechanical housings including hermetic and non-hermetic packages. Figure 3 provides a broad overview of the key packaging technologies required to produce most integrated photonic modules.

Current Challenges: Currently, the main challenge to be addressed is the ability to package photonic devices in large volumes and at costs that can meet market demands. Current photonic packaging processes typically rely on serial or device-level packaging of individual modules. Such processes have been in use for many years but are only viable for high-cost and low-volume applications such as advanced fiber optic telecommunication. However, with the rapid growth in applications such as datacenters and sensors for the Internet of Things, current packaging processes are incapable of meeting emerging market demands. This presents a critical manufacturing and cost bottleneck.

A major development in future packaging will be the transition from device-level to wafer-level packaging. Wafer-level packaging for photonic devices will leverage-off and more closely align with developments in electronic packaging, with the increased use of new substrates and interposers to co-package photonic and electronic devices in more compact sub-systems. Wafer-level packaging provides a route to improved scaling of the manufacturing process, ensuring packaging is economically viable, especially for mass market applications. As silicon photonics become a more widely used technology platform, the high-volume CMOS compatible assembly and packaging processes used in electronics manufacturing will become more common-place for photonic manufacturing. Such wafer-level packaging processes will start to be adopted during the next 5 years, becoming more standardised in 5-10 years.

Needs: New precision packaging equipment and tools will be required to implement these advanced manufacturing processes. There will be a greater use of automated and passive optical alignment processes using advanced machine vision and robotic systems, moving away from existing operator assembly processes. Operator driven assembly is not only unsuitable for very high-volume manufacturing but is also unsuited to delivering the sub-micron alignment tolerances required for complex multi-channel integrated photonic devices. Developments in this area will also benefit from advances made in packaging equipment used for advanced electronics assembly.

New materials will also be required to facilitate increasing demands for improved optical, electrical and thermal performance. For example, as photonic modules become more compact, there will be an increased demand to effectively manage heat dissipation though passive (non-thermoelectric) means. This will require new materials with improved thermal conductivities and which exhibit the extended lifetimes required for robust photonic modules. New materials will also be required to facilitate low-cost non-hermetic packaging

of photonic devices. Although non-hermetic, these encapsulation materials must act as a barrier to moisture ingression, have excellent thermal conductivities to dissipate heat from the package and impart minimum stress, ensuing long lifetimes in harsh operating environments.

As photonics becomes more pervasive, with increasing numbers of applications across a diverse range of markets, there will be a growing demand to develop co-packaging designs, incorporating photonics with electronics, MEMs and microfluidics. Healthcare presents the greatest opportunities for this technology trend. For example, point-of-care (PoC) diagnostics will require a photonic sensing platform to be co-packaged with microfluidics for sample delivery as well as electronics for in-situ signal analysis. PoC diagnostic devices have the potential to open mass consumer-driven markets, so wafer-level packaging will be essential to enable cost-effective devices.

Finally, the described developments will need to align more closely with design rules and standards. A coherent set of packaging design rules and standards ensures developments in new processes, materials and equipment ensuring future supply chains, from design and foundry, to packaging and test. Standard processes will allow the creation of training programs for manufacturing workforce and the reach of the real potential of integrated photonics, especially for emerging mass markets.

INTRODUCTION

Packaging of integrated photonics or photonic integrated circuits (PICs) is evolving. This evolution is driven by the emergence of new applications in markets that have extremely high-volume requirements, typically millions of components per year. Applications include, high-speed communications for data centers, sensors for automotive such as LIDAR, medical, and point-of-care diagnostics, and the growth of the Internet of Things (IoT).

There have been significant developments to realize cost-effective PIC device fabrication processes, but now there exists a packaging bottleneck that is impeding the growth of these markets. Key challenges to be overcome include: i) low-cost optical fiber and micro-optical packaging processes that provide high coupling efficiencies (e.g., <1 dB loss per optical interface), ii) the ability to package large numbers of optical channels per chip (e.g., >20 channels per optical interface), iii) the integration of different PIC platforms (e.g., Si, InP and SiN), and iv) the hybrid and heterogeneous integration of photonic and electronic devices in a common package. Challenges also remain in providing high-speed electrical packaging as required for communication systems with bandwidth requirements of >100 G. In addition, the drive to develop highly integrated photonic and electronic components in a single package adds to the difficulty of efficiently managing thermal loads. Critically, the technologies developed to overcome all these challenges must be implemented in high-volume manufacturing environments, using cost-effective materials and packaged using equipment that operates using automated machine vision (passive) alignment processes.

Existing photonic packaging processes typically rely on component-level packaging, where optical and electrical connections are assembled after the photonic device has already been placed in a mechanical package. This serial type process flow has limited throughput, and scale-up in manufacturing depends directly on the number of packaging machines. Historically, such serial process flows have been acceptable for low-volume high-value applications, such as fiber optic telecommunication that requires extremely high reliability and long lifetimes. The typical packaging for such a telecom component involves: 1) The photonic device assembled in the package; 2) Electrical connection using gold ribbon wire bonding; 3) Active alignment of the optical fiber to minimize insertion loss; and 4) Hermetic sealing of the mechanical housing in an inert atmosphere. This serial packaging approach, however, cannot meet the cost and volume demands of emerging mass markets in photonics. These packaging processes can account for most of the product manufacturing cost, making photonic device packaging prohibitively expensive for many emerging low-cost applications, see Figure 1.

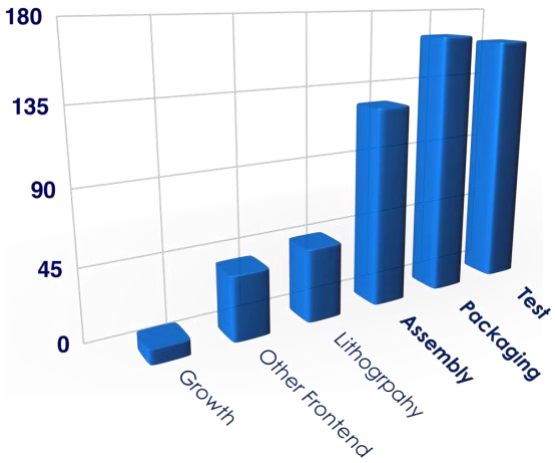


Figure 1: Breakdown of unit cost (US$) for an InP photonic device, showing that most of the product cost (> 75%) is dedicated to packaging and testing [Ref 1].

The advent of the PIC is helping to address the packaging bottleneck. For example, PICs offer many technological advantages, combining high levels of functionality in a single chip that can be applied across multiple markets, from communications to medical diagnostics and sensing. The high refractive index of the silicon optical waveguide results in a highly compact optical system, with dimensions on the order of 1 cm^2 or less. Critically, using silicon for photonics enables us to benefit from the well-established process flows and manufacturing equipment developed by the CMOS semiconductor industry. It is possible to use CMOS wafer-scale assembly and packaging processes to overcome the throughput limits of existing packaging processes, ensuring photonic systems meet the demands of emerging mass markets.

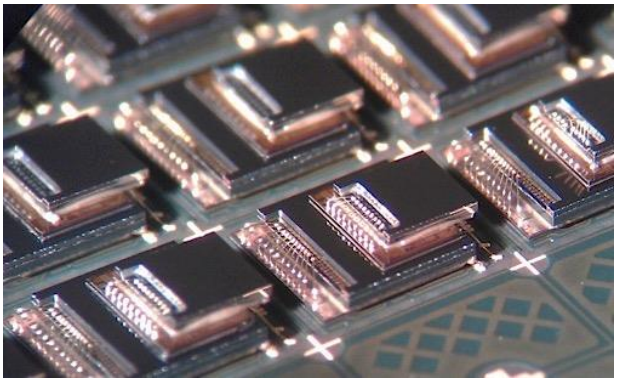


Figure 2: Future PIC packaging will require automated active and passive packaging processes at the wafer-level, moving away from serial or device-level processes. This includes packaging processes such as optical, electrical and mechanical or environmental encapsulation.

PIC packaging requires a wide variety of technologies which can result in a complex manufacturing process. Figure 3 shows a high-level organization chart giving a breakdown of the key PIC packaging technologies.

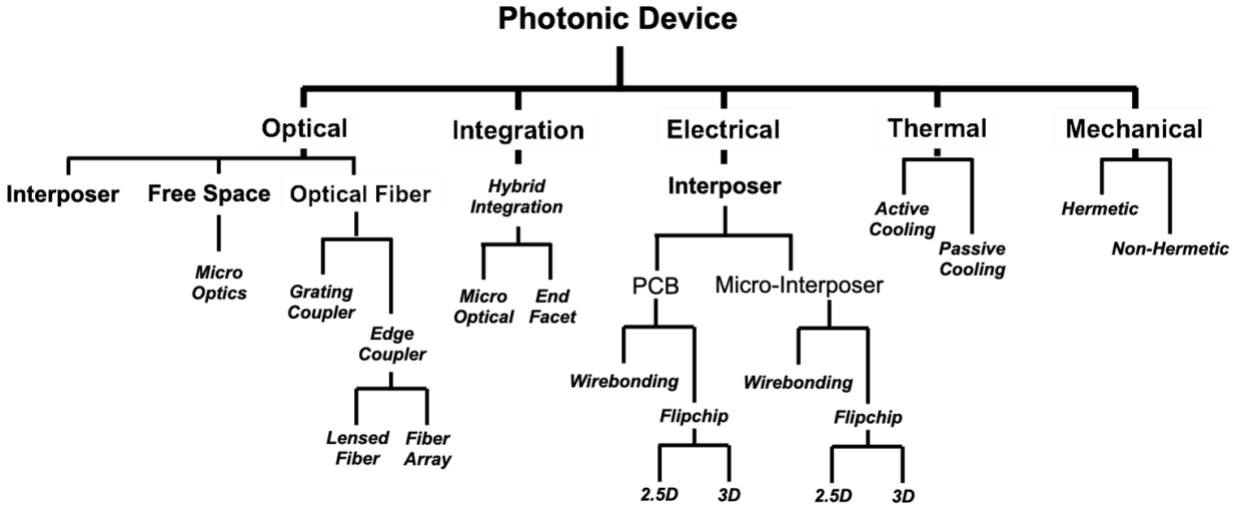


Figure 3: Organization chart showing the key packaging technologies, including; optical, integration, electrical, thermal and mechanical aspects.

An important guiding principle when considering the development of future PIC packaging technologies, is to ensure that suitable technologies are developed for all PIC platforms, including Silicon, InP and SiN. Furthermore, since packaging can contribute to most of the product cost, much greater collaboration will be required between PIC designers, foundries, packaging providers, equipment builders and application users.

The following sections provide a detailed overview of critical parts of the packaging roadmap, from design and materials, to optical and electrical interconnection technologies. Requirements for packaging

equipment and critical research needs are also addressed. Finally, emerging technology gaps and showstoppers are identified.

SITUATIONAL (INFRASTRUCTURE) ANALYSIS

The environment is rapidly changing and will require revolutionary changes after 50 years where the change was largely evolutionary. The major factors driving the need for change are:

- The end of Moore's Law scaling
- The emergence of 2.5D and 3D integration techniques for packaging
- The emerging world of the Internet of Everything causing explosive growth in the need for connectivity
- Mobile devices like smart phones and tablets are growing rapidly in number and in data communications requirements driving explosive growth in the required capacity of the global communications network
- Migration of data, logic and applications to the cloud drives demand for reduction in latency while accommodating this network capacity growth.

Satisfying these emerging demands cannot be accomplished with the current electronics technology and they are driving new and different integration approaches. The requirements for power, latency, bandwidth/bandwidth density and cost can only be accomplished by revolutionary change in the global communications network, all the components in that network and everything attached to it. Ensuring the reliability of this "future network" in an environment where transistors wear out will also require innovation in how we design and test the network and its components.

The transistors in today's network account for less than 10% of total power, total latency and total cost. The interconnection of these transistors and other components in the IC, in the package, on the printed circuit board and at the system and global network level is where the future limitations in performance, power, latency and cost reside. Overcoming these limitations will require heterogeneous integration of different materials, different devices (logic, memory, sensors, RF, analog, etc.) and different technologies (electronics, photonics, plasmonics, MEMS. etc.). New materials, manufacturing equipment and processes will be required to accomplish this integration and overcome these limitations.

MANUFACTURING EQUIPMENT

The development of equipment suitable for high-volume packaging is critical to the successful commercialization of PIC technologies. Significant developments have been achieved to develop electrical packaging equipment for processes such as 3D integration of electronics. The alignment tolerances required for these electrical packaging processes are typically in the range of 3-5 microns, which enables fast wafer-scale alignment and bonding processes. However, optical alignment typically requires sub-micron alignment tolerances, which can result in relatively slow processes, creating a significant bottleneck in the overall manufacturing process. To address this bottleneck, progress needs to be made in automation of fast load alignment and bonding of fiber and micro optical components. Faster computer vision (passive) processes need to replace the existing active steps. More precise vision systems combined with improved software algorithms and robotic systems for loading and unloading of packaging materials will have to be developed. In addition, equipment will have to accommodate wafer-scale packaging processes, where packaging and test can be more easily combined in fast process sequences.

Packaging equipment will also benefit from standardization of packaging processes, enabling standardization of equipment, similar to the co-development of device and equipment occurring in the microelectronics industry.

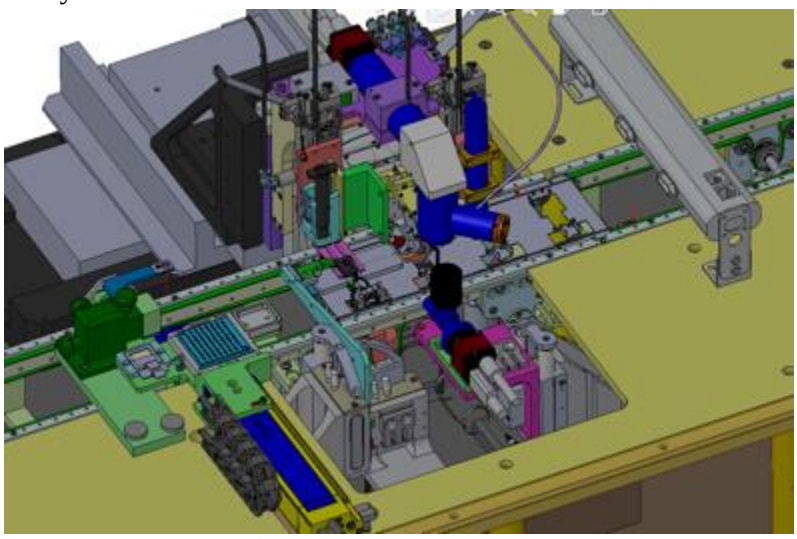


Figure 4: Packaging conveyer system for fast assembly of photonic components in package (image from Ficontec GmbH).

MANUFACTURING PROCESSES

Package/System Co-Design and Multiphysics Simulation

The packaging solutions for photonic circuits must incorporate heterogeneous integration of different materials and different circuit fabric types. This adds unique challenges due to the differences in the coefficient of thermal expansion, mechanical properties and operating temperature requirements. In order to avoid the cost and time associated with building and characterizing physical prototypes followed by a redesign cycle these experiments and design verifications must be done in the computer. This means co-design and simulation of optical, thermal, mechanical, electrical and, in some case, even chemical properties of the package. There are some CAD tools available today that partially address this need but there is nothing available today that is adequate. These tools must integrate across the boundaries from active and passive devices to full system level products as illustrated in Figure 5.

Tools for heterogeneous integration across boundaries of device, package, printed circuit board and product essential to migration to higher density (SoC, SiP, 2.5D, 3D, etc.) and time to market.

Electronics – Photonics – Plasmonics

This enables:

- ✓ Increased performance and bandwidth
- ✓ Decreasing latency, power, size, cost
- ✓ Reduced time to market

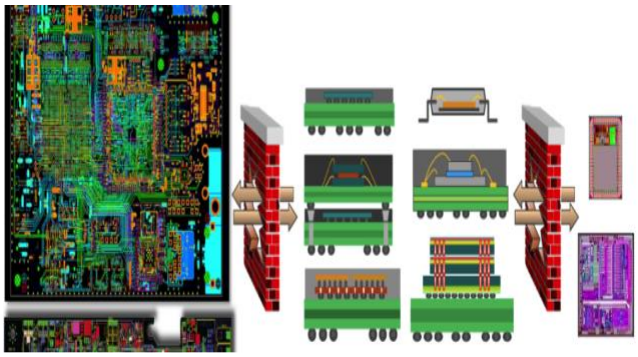


Figure 5: CAD Tools enabling design and simulation can prevent challenges from becoming roadblocks.

These tools and photonic/electronic spice modeling are critical for the design of monolithic photonic integrated circuits as well as the packaging for those circuits. The incorporation of as many of the system features as possible into a monolithic PIC is an important goal since it will address many of the difficult challenges such as cost, power, latency and performance. The accurate simulation of these monolithic photonic circuits will guide packaging by identifying requirements for:

- Thermal management and temperature control
- Stress management to reduce stresses imposed on the IC during the use case and thermal cycling
- Component placement accuracy both for initial assembly and changes incurred through thermal cycling in the use case.

CAD tools available today may meet the needs of early development phases, when the design is focused at improving the functionality of single devices without paying attention to system characteristics. The SiP packaging design tools do not yet support the heterogeneous and 3D integration that will be required to do the development and design verification in the computer. This will be essential for the short product life cycles and short design times associated with the portable consumer products. This is a very complex problem since simulation requires detailed materials properties that are not available. As layers in a device or a package for that device become thinner, the materials properties are increasingly determined by the interface rather than the bulk properties even when bulk properties are known.

This task is made more difficult as we incorporate new materials including composite materials with properties that are not well known. Even if we know bulk properties, the mechanical and electrical properties of very thin layers are controlled more by the interfaces to dissimilar materials than by bulk properties. Understanding the controlling properties for new materials and very thin layers of traditional materials is a difficult challenge. If that challenge is not met, we will have limited ability to optimize the design and construction of both the monolithic photonic circuits themselves and the packages that protect them without building and testing prototypes. This will not meet market requirements for cost or time to market.

The critical properties that must be known and taken into consideration in the design process are presented in Table 1 below.

Table 1: Critical Properties for Selected Materials.

Material	Critical Properties
Electrical Conductors	Conductivity in 3 dimensions over processing and use case temperature ranges which are application dependent
	CTE in 3D at processing and use case temperature ranges
	Bonding/joining characteristics
	Conductivity in 3 dimensions over use case temperature range which is application dependent
Thermal conductors	CTE in 3D at processing and use case temperature ranges
	Electrical conductivity
	Modulus
	Fracture toughness
	Interfacial adhesion
Insulators	Breakdown field strength
	CTE in 3D at processing and use case temperature ranges
	Fracture toughness
	Modulus
	Dielectric constant
	Leakage current

Table 1 addresses some of the packaging materials and the critical properties for those materials. There are many other materials and materials properties that must be considered.

These include:

- Active materials (both optical and electronic)
- Waveguide materials for optical signals
- Die attach materials
- Underfill materials
- Solders
- Mold compounds
- Composite materials that may be electrical/thermal conductors or insulators

Properties for each of these materials for both use case and processing temperatures must be known for the experiments and design verifications to be performed in the computer to save time to market and design cost.

Heterogeneous Integration

Heterogeneous Integration for packaging refers to the integration of separately manufactured components into a higher-level assembly (package) that, in the aggregate, provides enhanced functionality and improved operating characteristics. The components that will be assembled into the resulting complex 3D-SiPs may include:

- Monolithic PICs (incorporating photonics, electronics and plasmonics)
- Other discrete optical components that are not integrated in the photonic integrated circuits.
- Si based logic and memory ICs
- MEMS devices
- Sensors (including a growing list of photonic sensors)
- GaN power controller circuits
- RF circuits
- Compound (direct bandgap) semiconductor lasers
- Optical interconnects to and from the outside world
- Electrical interconnects to and from the outside world
- Passive components (including integrated passive devices)
- New devices and new materials that will enter the area over the life of this roadmap.
- Lithium Niobate

Each of these components has its own packaging requirements that must be satisfied which results in a variety of complex packages. The package designs should use standard equipment, materials and processes where possible to reach high volume for each design. This will be key to driving down cost and improving reliability.

The monolithic photonic integrated circuits will include active electrical, optical and probably plasmonic devices that must coexist and, where possible, be manufactured with common processing technology. The use of a common process to build electrical logic, memory, power controllers and plasmonics will inevitably result in compromises to the process for each of the circuit types. The monolithic circuits using a single process is enticing but the compromises increase cost and power while reducing performance. Historically this has resulted in a disaggregated structure with multiple packages and costly assembly processes. We need the performance, size and cost of monolithic ICs and we also need the performance and cost of using the optimal material and process for each function. These two “needs” cannot be satisfied with today’s mainstream technologies. Recent developments in wafer level packaging offer the promise of approaching this “best of both worlds” scenario. We can build each circuit fabric type with the optimal material and process and assemble it at wafer level thereby retaining much of the parallelism in manufacturing required to control cost. The wafer level packaging (WLP) technology also facilitates use of the third dimension; effectively reducing the physical distance between components which drives down power, latency and cost.

The increase in package substrate area for the SiP products, the historical processing temperatures that can range up to 400°C and the operating temperatures that are often limited to less than 100°C due to junction temperature limitations result in large stresses due to differential CTE between the package substrate and package contents. The result is warpage of the package substrate and/or components within the package. This issue will become more critical as we continue to decrease thickness of wafers, other package components and the layers of conductors and dielectrics in the package interconnect to manufacture thinner products.

This warpage results in assembly yield loss and may cause loss of mechanical stability required for photonic components. Even if we handle the warpage and assembly yield issues, the high processing temperature will result in substantial stresses built in at the lower use case temperatures. This is a yield and reliability limitation that must be addressed. It will become more important as the maximum junction temperature for logic and memory continues to drop to protect the sub-10 μm device geometries of the future.

This chapter will provide guidance to industry, academia and government identifying key technical challenges with sufficient lead time that they do not become roadblocks preventing the continued progress in data processing and communication that is essential to the future growth of the industry and the realization of the promise of continued positive impact on mankind. The approach is to identify the requirements for photonic packaging in the electronics industry through 2030, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions.

MATERIALS

Package Substrates

The dominate package substrate today uses organic laminate materials with limitations in mechanical stability, large CTE differential with silicon and limited wiring density. Today there are four different classes of material competing to be the package substrate of choice. They are:

Organic laminates
Organics have the lowest cost but have limitations in lack of mechanical stability, limited thermal conductivity and a large differential CTE with semiconductors. This material accommodates embedded active and passive components much easier than any other package substrate material. Composites of organic laminates are continuing to make progress but do not meet future needs for photonic packaging. It is the solution of choice for single chip CMOS packages.

Low temperature co-fired ceramics (LTCC)
This material has excellent mechanical stability, acceptable CTE match with semiconductors and good thermal conductivity but has limitations in wiring density, I/O pitch and cost. It is the solution of choice for harsh environments.

Glass
This material has advantages in high breakdown field strength, a true insulator which means essentially no leakage current and no variable capacitance. It does not match the bandwidth density of silicon and it has the worst thermal conductivity of candidate materials. There are several applications with low thermal density for which glass may eventually be the material of choice. There is a concerted effort to develop glass interposer technology for selected applications and it is likely that there will be high volume applications in the future where thermal density is not high. An example of the production flow for through glass vias (TGVs) is shown in Figure 6 below.

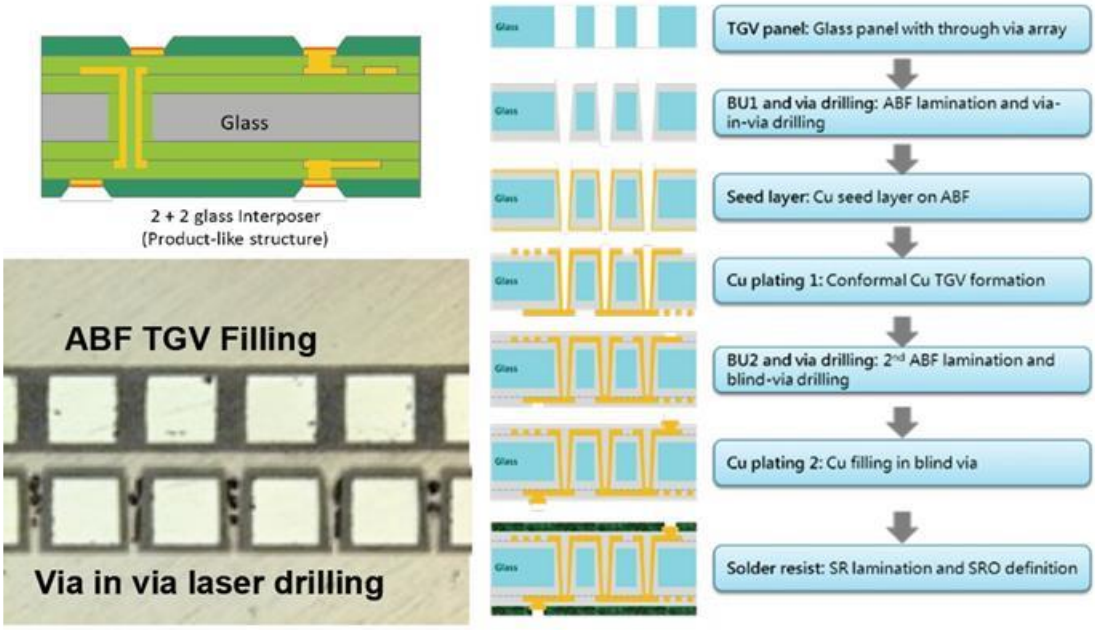


Figure 6: Glass TGV package substrate process flow.

Silicon

Silicon has excellent CTE match, excellent mechanical stability and the best wiring density. Its limitation is in cost. On a total cost per bandwidth basis, this limitation should be resolved as we come down the learning curve. It has better thermal conductivity than other package substrate materials with the exception of some of the LTCC materials. It also has the limitations of a being a semiconductor which means variable capacitance and lower breakdown field strength. It is rapidly becoming the solution of choice for package substrates with very high bandwidth requirements and it is the mainstay of the 2.5D integration currently in volume use for Field Programmable Gata Arrays.

New Packaging Materials

Conductors

The thermal and electrical conductors limit the improvements in power, performance, latency and cost. The state of the art of electrical interconnect today is copper with ultra-low κ dielectrics and for photonics it is active optical cables with multimode fibers. Both will have to change. The carbon-based materials show great promise as shown in Figure 7 below.

	Cu	CNT	GNR	
Max current density (A/cm^2)	~10^6	> $1x10^8$	> $1x10^8$	$x10^2$
Melting Point (K)	1356	**3800** (graphite)	**3800** (graphite)	
Tensile Strength (GPa)	0.22	22.2	23.5	$x10^2$
Thermal Conductivity ($\times10^3$ W/m-K)	0.385	1.75 *Hone, et al. Phys. Rev. B 1999*	3 - 5 *Balandin, et al. Nano Let., 2008*	x10
Temp. Coefficient of Resistance (10^{-3} /K)	4	< 1.1 *Kane, et al. Europhys. Lett.,1998*	-1.47 *Shao et al. Appl Phys. Lett., 2008*	
Mean Free Path @ room-T (nm)	40	> 1000 *McEuen, et al. Trans. Nano., 2002*	~ 1000 *Bolotin, et al. Phys. Rev. Let. 2008*	x25

Figure 7: Carbon conductor properties look better than copper. [left to right, top to bottom: 7, 8, 9, 10, 11, 12]

Despite the advantages in current density and both electrical and thermal conductivity there are many questions that must be answered before either carbon nanotubes or graphene can be considered as practical inter connect materials. The processes we use today for metal interconnects and heatsinks such as soldering, plating, lithographic patterning, TSVs, etc., do not yet exist for these conductors.

Composite conductors are showing more promise. The results to date for composite copper show good progress in both conductivity and current capacity and the theoretical performance is about three times the progress today as shown in Figure 8 below.

Composite Copper is in evaluation.

Current status:

Measurement	Conventional Copper	TeraCopper®
Resistivity (Ohm·cm)	1.66×10^{-6}	1.26×10^{-6}
Conductivity (S/m)	6.02×10^7	7.94×10^7
Increase in Conductivity	N/A	32%
Avg. Current Capacity(Amps/cm^2)	3.88×10^4	5.57×10^4
Increase in Current Capacity	N/A	44%

The first electrical performance improvement in copper since 1913 makes composite copper the most electrically conducting material known at room temperature.

Targets for improvement compared to conventional copper are:

- ✓ **100 % increase in electrical conductivity**
- ✓ **100% increase in thermal conductivity**
- ✓ **300% increase in tensile strength**

Source: NanoRidge

Figure 8: Materials properties for a Cu-carbon nanotube composite conductor.

The most important improvement with composite copper is in the dramatic reduction in coefficient of thermal expansion. In the use case temperature range the CTE ranges between 4 and 5.5×10-6/°C vs 17×10-6/°C for Oxigen-Free High thermal Conductivity copper. This has the promise of virtually eliminating stress and warpage due to differential thermal expansion which will be addressed in the package manufacturing processes section. The data on progress to date is shown in Figure 9 below.

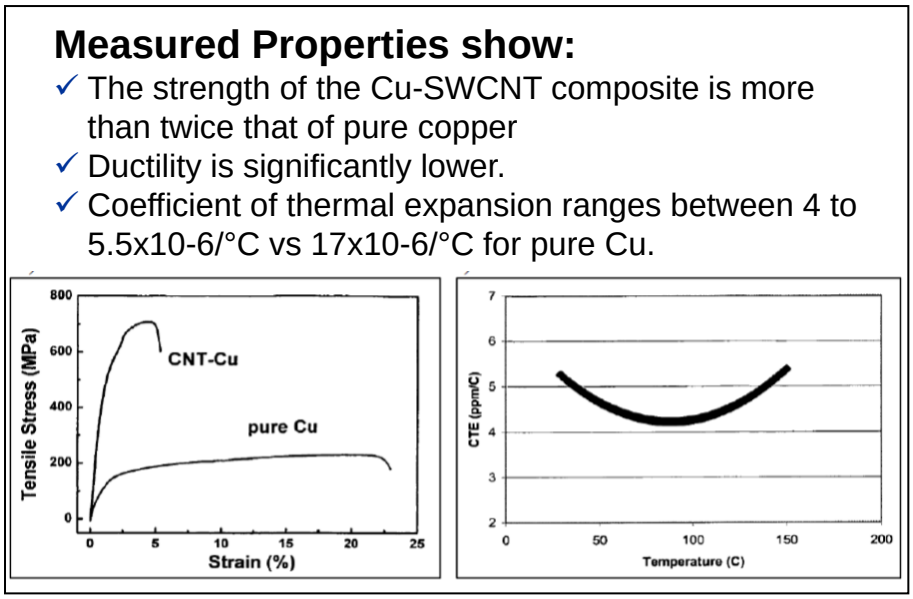


Figure 9: Coefficient of thermal expansion and tensile stress/strain comparison for OFHC and Composite copper.

Dielectrics

Low κ dielectrics have been in use for several years with substantial efforts continuing to reduce the dielectric constant. Although there has been some success, the practical dielectric constant still remains above 3 after processing for most of the candidate materials. There is a new generation of porous spin-on materials that have demonstrated dielectric constant below 2.0 but these materials are not yet fully qualified for production use.

Joining Materials

The joining/connecting materials in use today are primarily copper for interconnects either as wire bonds or copper pillars, soldering or layer to layer bonding using either thermal compression or a low temperature Direct Interconnect Bonding (DIB) process (patented by Ziptronix). The high reflow temperatures for lead free solders result in joining the layers at ~250°C which is approximately 150°C above the maximum use case temperature. This results in stress built in at the use case temperature. There are known solutions to this problem employed today. One is the use of nano-copper solder. This material was developed by Lockheed Martin and has been in use for space-based applications for several years. The temperature of the melting of the solder is reduced by the high surface energy of very small particles so that joining can be accomplished below 150°C. Data for this material is illustrated in Figure 10 below.

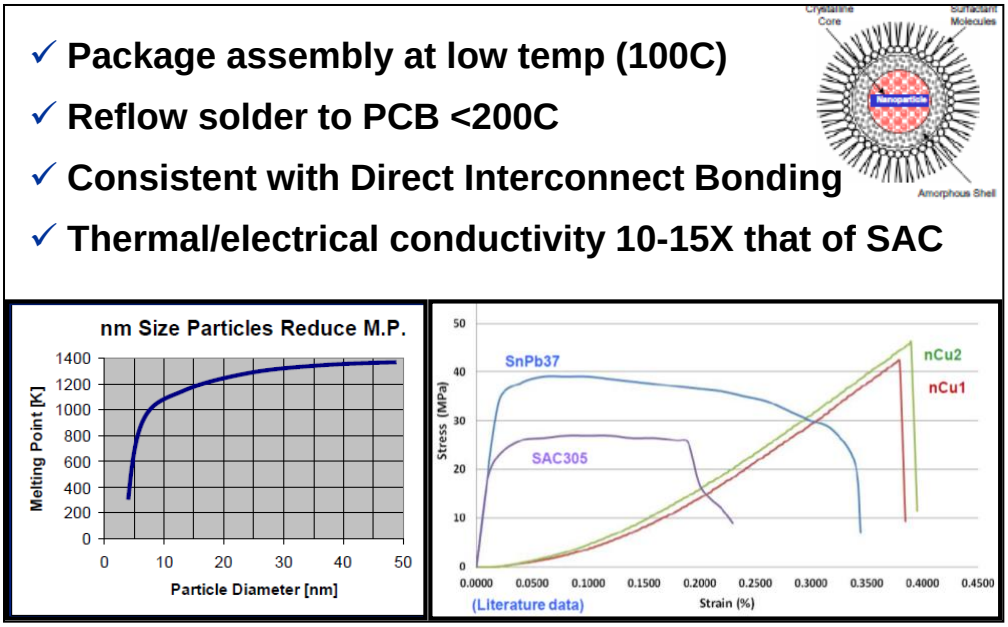


Figure 10: Properties of copper nano-solder, low processing temperature & improved conductivity.

There are other developments taking place for improved thermal conductivity and mechanical properties for polymer composites that will also support continued progress for the electrical, thermal, optical and mechanical properties of advanced packaging that are not addressed in this Roadmap. The material above outlines in large part the current state of the art for electronics packaging that will be adopted for photonic/electronic SiP packages of the future.

QUALITY/RELIABILITY

To be determined

ENVIRONMENTAL TECHNOLOGY

To be determined (ROHAS, Low temperature TinBismut & In based soldering)

TEST, INSPECTION, MEASUREMENT (TIM)

To be determined

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS

SILICON INTERPOSER

The introduction of the silicon interposer has changed the package substrate for the most advanced packaging to silicon. This technology has been known for many years but was not adopted due to high cost. At the leading edge the interconnect density available using obsolete manufacturing equipment for 90-65 nm node ICs became cost effective for very high bandwidth interconnect. Silicon has the further advantage of embedding optical waveguide in the silicon substrate for heterogeneous integration of photonics, electronics and plasmonics into a single package. There are 2 tables following that address the Silicon package substrates and the organic package substrates. There are no tables included for the other package substrate types since at present the other two seem to be limited to lower volume specialty packages. Table 2 below shows the critical parameters for the package substrate through 2030.

Table 2: Package Substrates for Heterogeneous Integration: High Performance, High End.

Year of Production		*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2027*	*2028*	*2029*
Parameter	**unit**														
Package Type	-	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA	S-BGA
Interconnect Method	-	FC+TSV	FC+TSV	FC+TSV	FC+TSV	TSV	TSV	TSV	TSV	TSV	TSV	TSV	TSV	TSV	TSV
Chip to Substrate Interconnect Land Pitch	µm	120	110	110	110	110	100	100	100	100	90	90	90	90	90
Max. Pin Counts	#	4000	400	5300	5300	6500	6500	6500	6500	6500	7000	7000	7000	7000	7000
Typical Pin Counts	#	4000	400	5300	5300	6500	6500	6500	6500	6500	7000	7000	7000	7000	7000
Min. External I/O Pitch	mm	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
Typical External I/O Pitch	mm	0.65	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
Typical Materials	-	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon
Typical Buildup Materials	-	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	SiO_3	SiO_4	SiO_5
Max. Layer Counts	#	4+2	4+2	4+2	4+2	4+2	6+2	6+2	6+2	6+2	6+2	6+2	6+2	6+2	6+2
Typical Layer Count	#	4+2	4+2	4+2	4+2	4+2	6+2	6+2	6+2	6+2	6+2	6+2	6+2	6+2	6+2
Min. Finished Substrate Thickness	mm	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Typical Finished Substrate Thickness	mm	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Core Material Tg	°C	1410	1410	1410	1410	1410	1410	1410	1410	1410	1410	1410	1410	1410	1410
Core Material CTE (X-Y)	ppm/°C	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Core Material CTE (Z)	ppm/°C	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Core Material Dk@1GHz	-	12	12	12	12	12	12	12	12	12	12	12	12	12	12
Core Material Df@1GHz	-	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005	0.0005
Core Materials Young's Modulus	Gpa	185	185	185	185	185	185	185	185	185	185	185	185	185	185
Core Material Water Absorption	%	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Buildup/RDL Material Tg	°C	700	700	700	700	700	700	700	700	700	700	700	700	700	700
Buildup/RDL Material CTE (X-Y)	ppm/°C	3	3	3	3	3	3	3	3	3	3	3	3	3	3
Buildup/RDL Material CTE (Z)	ppm/°C	16	16	16	16	16	16	16	16	16	16	16	16	16	16
Buildup/RDL Material Dk@1GHz	-	2.0	2.0	2.0	2.0	1.8	1.8	1.8	1.6	1.6	1.6	1.6	1.6	1.6	1.6
Buildup/RDL Material Df@1GHz	-	0.003	0.003	0.003	0.003	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001	0.001
Buildup/RDL Materials Young's Modulus	GPa	10	10	10	10	10	10	10	10	10	10	10	10	10	10
Buildup/RDL Material Water Absorption	%	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Min. Line width/Space	µm	5/5	3/3	3/3	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
Min. Conductor Thickness	µm	5	5	5	3	3	3	3	3	3	3	3	3	3	3
Min. Through Via Diameter	µm	80	80	70	70	70	70	60	60	60	55	55	55	55	55
Min. Through Via Land Diameter	µm	150	150	150	150	150	150	120	120	120	110	110	110	110	110
Min. Micro Via Diameter	µm	30	30	30	30	30	30	30	30	30	30	30	30	30	30
Min. Micron Via Land Diameter	µm	60	60	60	60	60	60	60	60	60	60	55	55	55	55
Min. Through Via Pitch	µm	275	275	250	250	250	250	250	250	250	250	220	220	220	220

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Notes

1. After 2015, Core Materials will be changed to MEMS based cooling device which will use micro fluidic.

2. After 2017 silicon wve guides will be used for optical signal interconnect

2. There are several parameters that do not change over the period covered by the Roadmap. They are:

Max. Body Size	*mm×mm*
Typical Body Size	*mm×mm*

4. State of the art materials may not be compatible with cost requirements for volume production

5. Water absorption test is: JIS C6481

ORGANIC INTERPOSER

In some cases, based on warpage considerations and/or minimum pitch on a PCB where the package is to be mounted on a combination of both a silicon substrate (interposer) and an organic package substrate are employed between the active devices, the silicon interposer may be mounted on a lower cost organic package substrate with a larger pad pitch. Figure 11 below illustrates this architecture which is in high volume production today.

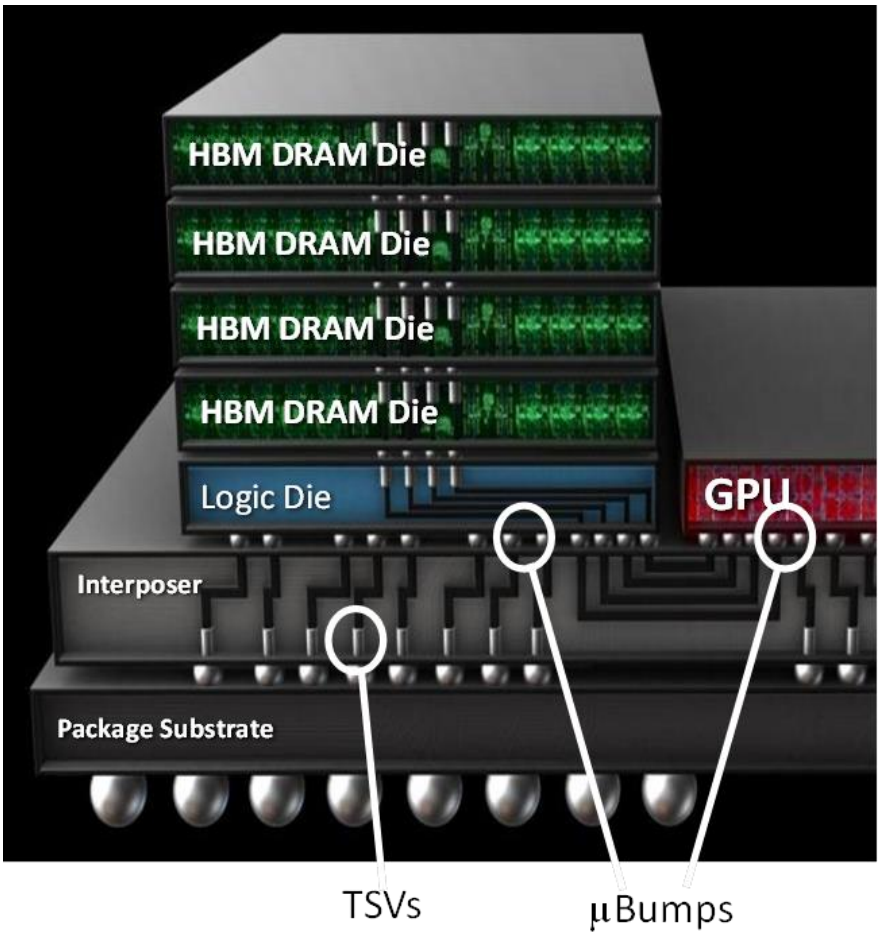


Figure 11: 3D-Sip Package using Silicon Interposer and Organic Package Substrate (Source AMD).

The example above illustrates the use of a silicon interposer as a substrate for logic, memory and a graphics processor connected by µbumps to the interposer. The organic package substrate is joined to the interposer through silicon vias (TSVs) with solder balls. The entire image constitutes a ball grid array (BGA) package with large solder balls on the bottom for connection to a system level printed circuit board. This product is the Fiji graphics processor from AMD and the package is in high volume production today. It represents the state of the art for 3D SIP packaging in 2015 with more recent developments increasing the interconnect density and adding optical waveguides within the package substrate.

The characteristics of this organic package substrate used for mounting the silicon interposer are listed in Table 3 below.

Table 3: Organic Package Substrates: For mounting Silicon Interposer and other SiP components for Heterogeneous Integration.

Year of Production		*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*	*2029*	*2030*
Parameter	**unit**																
Chip to Substrate Interconnect Land Pitch	µm	100	100	95	95	95	95	95	95	95	90	90	90	90	90	85	85
Min. Finished Substrate Thickness	mm	1.1	1.1	0.8	0.8	0.8	0.8	0.6	0.6	0.6	0.6	0.5	0.5	0.5	0.5	0.5	0.5
Core Material Tg	°C	210	210	210	210	210	210	210	210	210	210	210	210	210	210	210	210
Core Material CTE (X-Y)	ppm/°C	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
Core Material CTE (Z)	ppm/°C	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10
Core Material Dk@1GHz	-	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
Core Material Df@1GHz	-	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007	0.007
Core Materials Young's Modulus	GPa	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24
Core Material Water Absorption	%	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07	0.07
Buildup Material Tg	°C	210	210	210	210	210	210	210	210	210	210	210	210	210	210	210	210
Buildup Material CTE (X-Y)	ppm/°C	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
Buildup Material CTE (Z)	ppm/°C	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40
Buildup Material Dk@1GHz	-	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
Buildup Material Df@1GHz	-	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013	0.013
Buildup Materials Young's Modulus	GPa	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
Buildup Material Water Absorption	%	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Min. Line width/Space	µm	10/10	8/8	8/8	5/5	5/5	3/3	3/3	2/2	2/2	1/1	1/1	1/1	1/1	1/1	1/1	1/1
Min. Conductor Thickness	µm	15	12	12	10	10	5	5	4	4	3	3	3	3	3	2.5	2.5
Min. Through Via Diameter	µm	80	70	70	70	70	70	70	60	60	60	55	55	50	50	50	50
Min. Through Via Land Diameter	µm	200	150	150	150	150	150	150	120	120	120	110	110	100	100	100	100
Min. Micro Via Diameter	µm	50	50	30	30	30	30	20	20	20	20	20	20	15	15	15	15
Min. Micron Via Land Diameter	µm	100	100	70	70	70	70	50	50	50	50	50	50	40	40	40	40
Min. Through Via Pitch	µm	275	275	275	250	250	250	250	250	250	250	250	250	220	220	220	220
Min. Solder Mask Openning	µm	60	50	50	50	50	40	40	30	30	30	25	25	20	20	20	20
Min. Solder Mask Openning Tolerance	µm	18	15	15	15	15	10	10	8	8	8	8	8	6	6	6	6

Manufacturable solutions exist, and are being optimized	
Manufacturable solutions are known	
Interim solutions are known	
Manufacturable solutions are NOT known	

Notes

1. The package type for this table is P-BGA

2. The interconnect method for this package is flip chip

3. There are several parameters that do not change over the period covered by the Roadmap. They are:

Max. Body Size	*mm×mm*
Typical Body Size	*mm×mm*
Max. Pin Counts	*#*
Typical Pin Counts	*#*
Min. External I/O Pitch	*mm*
Typical External I/O Pitch	*mm*
Typical Core Materials	*-*
Typical Buildup Materials	*-*
Max. Layer Counts	*#*
Typeical Layer Count	*#*

4. State of the art materials may not be compatible with cost requirements for volume production

5. Water absorption test is: JIS C6481

The Roadmap assumes that there will be no need for significant changes in geometries for this category since the first level of I/O count reduction and pitch translation will take place on the silicon interposer.

OPTICAL PACKAGING/INTEGRATION

Optical packaging typically involves bonding of optical fibers to the PIC device, where single or fiber arrays can be used. The conventional packaging process uses an active alignment procedure where the coupled optical power is continuously measured and maximized, and the fiber is fixed in position using a laser welding or UV epoxy curing process—sub-micron alignment tolerances are required. This process is performed at the component or package level, and suffers from significant throughput limitations, with cycle times on the order of minutes to tens of minutes per package, depending on the complexity of the photonic device to the assembled. Wafer-level packaging has the ability to overcome these limitations, where parallel alignment processes can achieve significantly higher throughputs: seconds per device. Eliminating the need to bond fibers to the photonic chip through the use of micro optics assembled on-wafer offers one solution. Using micro optics to produce an expanded and collimated beam enables the package to be used for free-space and pluggable fiber connectors. Furthermore, the package can be designed in a Surface Mount Technology (SMT) PIC style package, for example, a Dual-in-Line (DIL) or Ball Grid Array (BGA) design. SMT is the most widely used, cost-effective and standardised package in the

electronics world and could become a new standard for cost-effective PIC packaging. The SMT approach facilitates Module Integration or System-in-Package (SiP) of PICs. This style of optical interconnect is ideal for low-cost photonic packages, such as pluggable transceivers for data centers or disposable biosensors for medical diagnostics [Ref 2]. This type of high-volume and low-cost interconnect will become a viable alternative to the dominant fixed-fiber design, see Figure 12.

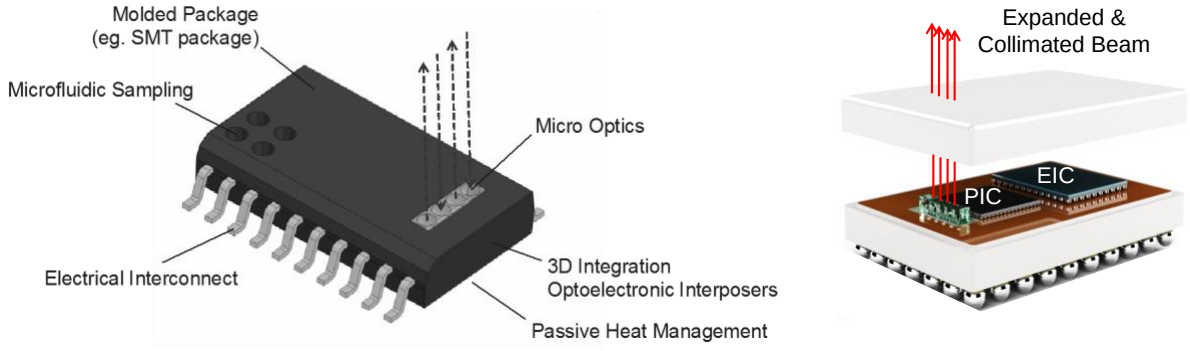


Figure 12: Concept of the fiber-less package with free space micro optics assembled at wafer-scale level. This type of package suits emerging low-cost applications, including datacenters and disposable biomedical sensors. Low cost Dual-In-Line (DIL) style surface mount package (left) and Ball Grid Array (BGA) style surface mount package (right). These SMT style packages have expanded and collilamted beams, suitable for both free-space and fiber array connectors. These designs may use out-of-plane optical couplers incorporating micro optics with integrated micro turning mirrors.

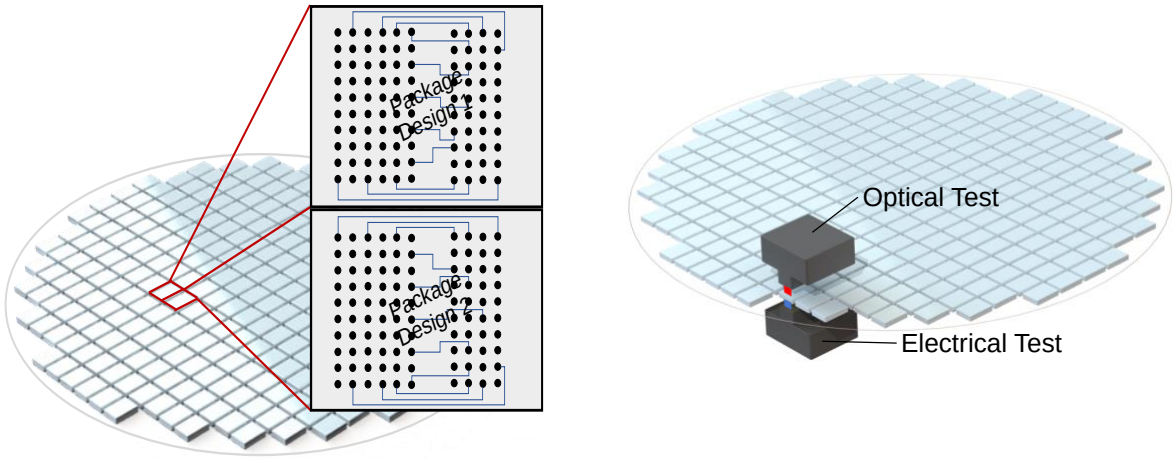


Figure 13: Wafer-level packaging, such as the surface mount (SMT) approach described above can enable the development multiple user designs on a single wafer, where the base wafer is used as package substrate and electrical interposer for co-packaging of photonic and electronic devices (left). This approach enables multi project packaging runs (similar to MPW device runs in wafer foundries) and wafer-level testing (right).

Although fiber attachment is expected to remain a key optical packaging process, it must be modified to reduce cycle time and make it more cost-effective. One approach is to use evanescent coupling. In this design, light is coupled between the optical fiber and PIC waveguide via an optical interposer, much like an electrical interposer is used to interface between adjacent electronic devices. Structuring the PIC at the wafer-level to include an evanescent coupling element is relatively straightforward, and when bonded on top of the optical interposer via a flip-chip process, enables light to efficiently transfer between the PIC and interposer waveguides. An added advantage of the evanescent technique is the ability to form an optical connection at any point on the PIC surface, rather than at the PIC edge or facet, as with standard fiber

coupling. Optical interposers can be fabricated in glass, with embedded waveguides interfacing between the optical fibers and PIC [Ref 3]. Although at a relatively early stage of development, both micro-optics and evanescent coupling indicate the benefits of using wafer-level processes to ease the burden of optical packaging.

Table 4: 5, 10- and 15-year roadmap challenges to be addressed for PIC optical packaging. This includes optical fiber, micro optical packaging and optical interposer packaging.

Technology	Coupling	Process *Current*	Performance *Current*	Process *+5 Years*	Performance *+5 Years*	Process *+10 Years*	Performance *+10 Years*	Process *+15 Years*	Performance *+15 Years*
Fiber-to-PIC*	*Grating*	DL / AA / 10µm	>2dB/facet	DL / **PA** / 10µm	>2dB/facet	DL / **PA** / 10µm	>0.5dB/facet	DL / **PA** / 10µm	>0.5dB/facet
	Edge	DL / AA / 3µm	>2dB/facet	DL / AA / 6µm	>1dB/facet	DL / **PA** / 10µm	>0.5dB/facet	DL / **PA** / 10µm	>0.2dB/facet
µOptics-to-PIC**	*Grating*	DL / AA / 10µm	>2dB/facet	**WL** / **PA** / 10µm	>2dB/facet	**WL** / **PA** / 10µm	>1dB/facet	**WL** / **PA** / 10µm	>0.5dB/facet
	Edge	DL / **PA** / 3µm	>2dB/facet	DL / **PA** / 3µm	>1dB/facet	**WL** / **PA** / 3µm	>1dB/facet	**WL** / **PA** / 3µm	>0.5dB/facet
Interposer-to-PIC***	*Edge*	DL / AA / 10µm	>1.5dB/facet	DL / **PA** / 10µm	>1dB/facet	DL / **PA** / 10µm	>0.5dB/facet	DL / **PA** / 10µm	>0.2dB/facet
	Evanescent	R&D Prototypes Only		Interposer foundry processes		Electro-Optic Interposers		RF-Electro-Optic Interposers	

Key: DL - die-level assembly; AA - active alignment process; WL - wafer-level assembly; PA - passive alignment process (machine vision); Xµm - MFD of the coupling mode; Fiber-to-PIC does not develop beyond DL, because the FA is typically much larger than the PIC
** Interposer-to-PIC does not develop beyond DL, because interposer is typically much larger than the PIC
*** The path to WL direct-writing of µOptics on the PIC-edge is clear; The process for singulation after µOptic growth needs development.

Critical Milestones: 1) Large volumes of PIC chips available within 5 Years to enable development of standardized high-volume packaging processes. 2) Low loss edge and grating coupling structures on wafer, ideally matched to standard fiber core dimensions, with a 5- to 10-year timeframe 3) Development of suitable high-volume fiber packaging equipment based on standardized packaging processes.

Regular Milestones: 1) Development plan to continuously reduce optical coupling losses for both edge and grating coupled PICs [<0.5 dB within 10 years]. 2) Development plan for wafer-scale packaging of micro optics on PIC to enable fiber-less packaging, for pluggable and disposable PIC packages.

Desirable Milestones: 1) Fiber-less package using micro optics for both grating and edge coupled PICs. 2) Integrated optical and electrical interposer on single or common material platform.

ELECTRICAL PACKAGING/INTEGRATION

Electrical packaging for photonics is often overlooked but can be the largest contributor to material costs within the package. As the demand for higher operating frequencies rises, there is a need to integrate the electronics closer to the PIC. In some cases, electronic and photonic functionality can be integrated in the same device, although hybrid integration using 2.5 and 3D integration processes tend to be the preferred technology [Ref 4]. Several photonic foundries now offer copper pillar processes, enabling electronic ICs, such as modulators and amplifiers chips, to be directly integrated into the PIC. This close integration supports extremely high-frequency operation of the photonic-electronic system. However, unlike an electronic system, photonic devices can be severely impacted from heat generated by the electronic chip, especially if the photonic device has wavelength sensitive functions such as switches, multiplexer and demultiplexer elements. 2.5D integration can alleviate this problem as it can thermally isolate devices. They also offer the potential to combine both optical and electrical functionality in the same interposer. If a glass interposer is used, optical waveguides can be defined in the glass substrate using processes such as femto-second laser inscription or ion diffusion to modify the local refractive index [Ref 5]. This type of dual functioning interposer is under development by several academic and industrial research groups and is

expected to become a commonly used technology for PICs that have complex electrical and optical functionality.

Table 5: 5, 10- and 15-year roadmap challenges to be addressed for PIC electrical packaging.

Technology	Process	Tech Lvl. *Current*	Materials *Current*	Tech Lvl. *+5 Years*	Materials *+5 Years*	Tech Lvl. *+10 Years*	Materials *+10 Years*	Tech Lvl. *+15 Years*	Materials *+15 Years*
3D Integration	Interface	DL / **PA**	50µm SBs	**WL** / **PA**	25µm SBs	**WL** / **PA**	<20µm CPB	**WL** / **PA**	<10µm CPB
(EIC-on-PIC)	Flip-Chip	DL / **PA**	±5µm Tol	**WL** / **PA**	±2.5µm Tol	**WL** / **PA**	±2µm Tol	**WL** / **PA**	±1µm Tol
2.5D Integration*	Interface	DL / **PA**	50µm SBs	DL / **PA**	25µm SBs	DL / **PA**	<20µm CPB	DL / **PA**	<10µm CPB
(EIC&PIC on Carrier)	Flip-Chip	DL / **PA**	±5µm Tol	DL / **PA**	±2.5µm Tol	DL / **PA**	±2µm Tol	DL / **PA**	±1µm Tol
PIC-on-Interposer**	Electrical	DL / AA	±1µm Tol	DL / AA	±2.5µm Tol	DL / **PA**	±5µm Tol	DL / **PA**	±10µm Tol
(Electro-Optic)	Optical								

Key: DL - die-level assembly; AA - active alignment process; WL - wafer-level assembly; PA - passive alignment process (machine vision); Xµm - MFD of the coupling mode;
*2.5D Integration does not develop beyond DL, because carrier dimension is large compared to PIC and EIC footprint; WL assembly not useful
**Here, the alignment tolerance is dictated by the WG-size and index-contrast in interposer; As technology matures tolerance will relax.

Critical Milestones: 1) 3D electrical interposers for high speed packaging for dense PIC circuits. 2) Fine pitch 3D electrical interposers for dense PIC circuits [20 micron interposer vias by 5 Years]. 3) Low cost electrical interposer materials with high speed performance [>50 GHz by 10 Years]. 4) Critical electronics assembled in-package.

Regular Milestone: Development plan to continuously increase the number of DC and RF lines and maximum operating channel frequency.

Desirable Milestone: Integrated optical and electrical interposer on single or common material platform.

THERMO-MECHANICAL PACKAGING

The typical operating temperature range of electronic devices is broad. *Altera-Intel* rate their "commercial" grade electronic-ICs as being operable from 0-85 ºC, and their "industrial" grade components from -40 to 100 ºC. Photonic devices are typically one order of magnitude more sensitive to temperature effects than electronics, and so require proportionately more sophisticated thermal management to remain "in spec". For example, the channel-spacing in DWDM systems is approximately 1nm, and the tuning coefficient of a typical µRing resonator on a Si-PIC is 0.1 nm/K, which means that a temperature change of just 10 ºC can result in channel-hopping. Currently, two approaches – passive-cooling and active-cooling – are used for photonic thermal management. Passive-cooling involves creating a low thermal-resistance path from the PIC to the module-housing for external conductive/convective-cooling, is relatively straightforward, and requires no additional power, but the PIC temperature ultimately-depends on the temperature of the module-housing. Future improvements to passive cooling depend on optimization of module designs (modelling and simulation), and access to new housing and bonding materials (e.g. plastic enclosures and graphene-based epoxies) to reduce the cost of the packaged photonic modules, while increasing their thermal performance. Active-cooling involves inserting a thermo-electric cooler (TEC) between the PIC and module-housing (which brings an unwanted increase the thermal resistance) and adding both a thermistor and control circuit to power the TEC, which then allows the PIC temperature to be set independently of the module-housing. Future improvements to active-cooling depend on improving the coefficient of performance of the TEC through better footprint-matching to the PIC, and optimized module

design and adopting new materials, as well as hybridization with passive-cooling strategies to reduce the power-budget for driving the TEC.

Table 6: 5-, 10- and 15-year roadmap challenges to be addressed for PIC thermal and mechanical packaging.

Technology	Coupling	Current	+5 Years	+10 Years	+15 Years
Active Cooling	*Materials*	Standard TECs & Contollers	Customized TECs & Controllers	µTECs matched to PIC-footprint	TEC material grown at **WL** on back-side of PICs
	Assembly	DL / **PA** / ±500µm	DL / **PA** / ±250µm	DL / **PA** / ±100µm	
Passive Cooling	*Materials*	Al Heat-Spreaders & Stnd Epoxy	Graphene-based materials	Direct Integration of PIC onto Wall of Module-Housing	Direct Integration of PIC onto Wall of Module-Housing
	Assembly	DL / **PA** / ±500µm	DL / **PA** / ±250µm		
Module Housing	*Comms.*	Gold-Box (Lead-type)	Gold-Box (Via-connections)	Plastic Box (RF-screening)	Plastic Box (RF + µOptic Interface)
	Sensing	Plastic Box (Custom)	Plastic Boxes (Standard-FF)	Standard-FF Boxes + µOptics	Standard-FF Boxes + µOptics

Key: DL - die-level assembly; WL - wafer-level assembly; PP - Pick & Place Process; ±Xµm - Tolerance of PP; FF - Form Factor; RF - Radio Frequency.

Critical Milestones: 1) New low-cost thermal interface materials for high-density PICs. 2) Develop thermal management approaches to eliminate the active cooling. 2) Low cost plastic PIC packages for emerging mass-market applications such as disposable biosensing. 3) Non-hermetic packages for non-telecom applications. 4) At the foundry/design-level, optimize PIC components for intended temperature of operation, rather than room-temperature, to reduce operating power-budget. 5) Hybrid approach to thermal management, where active TE-cooling is used only for stabilization, and passive-cooling to set base temperature.

Regular Milestones: 1) Development plan to reduce the need for in-package active PIC cooling. 2) Roadmap for standardization of PIC packages and packaging design kit (packaging PDK). 3) Realistic goals for incremental improvements to the CoP for active cooling. 4) Phased transition from Al/Cu heat-sinks and Ag-based thermal epoxies to more economic thermal-sinking materials, i.e. graphene-based epoxies.

Desirable Milestones: 1) Passive cooling using novel thermal interface materials (10 Years). 2) Integration of thermal energy harvesting devices to support control of PIC devices in-package. 3) 3D printing of packaging components for off-the-shelf packages [>10 Years]. 4) Identify a credible path for the integration of a thermal photonic materials and components into the process-flow of the photonic-foundries.

CRITICAL (INFRASTRUCTURE) ISSUES

WAFER LEVEL PACKAGING

Wafer level packaging (WLP) has been defined as a technology in which all of the IC packaging process steps are performed at the wafer level. The original WLP definition required that all package I/O terminals be continuously located within the chip outline (fan-in design) producing a true chip size package. This definition described a Wafer Level Chip Scale Package, with the processing of a complete wafer. From a systems perspective, under this definition, the limitation on WLP was how many I/O could be placed under the chip and still have a board design that can be routed.

Products coming to market today have more I/O than can be accommodated within the chip outline. The increased I/O density requires new packages known as “Fan-out” WLP (FOWLP). They are processed by placing individual sawn die into a polymer matrix that has the same form factor as the original silicon wafer. These “Reconstituted” artificial wafers are then processed through all of the same processes that are used for “real” wafers, and finally sawn into separate packages. Die are spaced in the polymer matrix such that

there is a perimeter of polymer surrounding each placed die. This area is used during redistribution layers to "fan out" the redistribution layers to an area larger than the original die.

This allows a standard WLP solder ball pitch to be used for dies that are too small in area to allow this I/O pattern without "growing" the die to a larger size.
WLP technology includes:

- Wafer level chip size packages (WLCSP)
- Fan-out wafer level packages
- Wafer capping
- Thin film capping for MEMS devices
- Wafer level packages with Through Silicon Vias
- Wafer level packages with Integrated Passive Devices
- Wafer level substrates featuring fine traces and embedded integrated passives
- Multi-die and 3D packages using FOWLP processes

There is wafer to wafer stacking technologies that will support stacked die WLP for future products including heterogeneous integration of electronic ICs and PICs. These technologies represent solutions to cost, power level, performance and size challenges for electronic/photonics products in the future.

WLCSP are mainly being used in portable consumer markets where small size, thickness, weight, and electrical performance are additional advantages to cost. Major trends include work for cost efficient rerouting with multi-layer RDL and improved design and simulation tools for WLP technologies.

With the introduction of TSVs, IPDs, Fan-out, and MEMS packaging technologies, WLP products can be used in a much broader range of applications, with higher I/O counts, and greater functional complexity. These packaging technologies open new opportunities for WLPs in the packaging field. Figure 14 below shows a variety of FOWLP types currently in production.

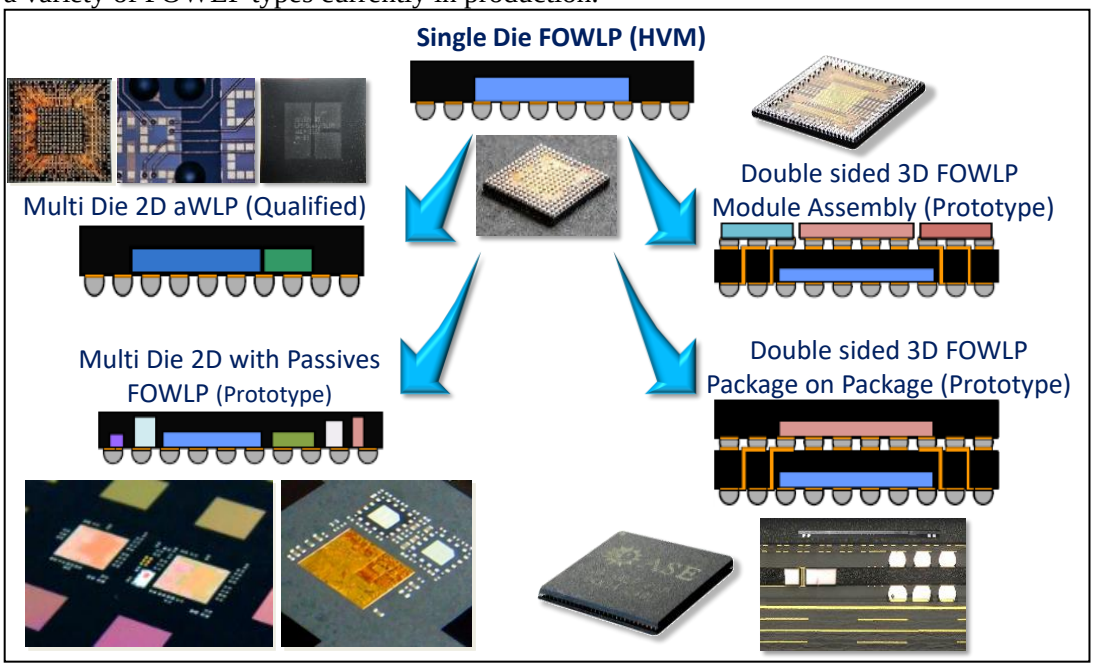
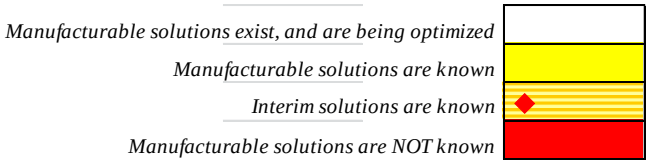


Figure 14: FOWLP in production qualification or production in 2015.

Table 7: Critical Parameters for Wafer Level Packaging through 2030.

Year of Production	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*	*2027*	*2028*	*2029*	*2030*
Cost per Area for Contract Assembly [1,2] (Cents/mm^2)																
a. Standard Logic and Analog/Linear – Low End	0.11	0.1	0.1	0.09	0.09	0.08	0.08	0.07	0.07	0.06	0.06	0.06	0.05	0.05	0.05	0.05
b. Standard Logic and Analog/Linear – Cost Performance	0.23	0.22	0.21	0.2	0.19	0.18	0.17	0.16	0.15	0.14	0.14	0.14	0.13	0.13	0.13	0.13
c. Standard logic, Analog and Photonic	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
d. Wafer Level Fanout	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Package size (mm^2) Including fan out and multi-die packages																
a. WLCSP- Memory	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250	20/250
b. WLCSP-Standard Logic and Analog/Linear	0.25/16	0.20/16	0.18/17	0.16/17	0.14/18	0.12/19	0.11/20	0.10/21	0.10/22	0.09/22	0.09/23	0.09/23	0.08/24	0.08/24	0.08/24	0.08/24
c. WLCSP- Wireless: Bluetooth, FM, GPS, WIFI	0.25/39	0.20/41	0.18/41	0.16/41	0.14/46	0.12/46	0.11/46	0.10/48	0.10/48	0.09/48	0.09/48	0.09/48	0.08/50	0.08/50	0.08/50	0.08/50
d. Wafer level fanout	2/144	2/144	1.8/156	1.8/156	1.6/169	1.6/169	1.5/182	1.5/182	1.5/182	1.4/196	1.4/196	1.4/210	1.4/211	1.4/212	1.4/213	1.4/214
Number of RDL Layers per side																
a. All WLP	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
UBM Thickness (µm)																
a. Standard Logic and Analog/Linear (low power)	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm	1.5–50 µm
b. Standard Logic and Analog/Linear (high power)	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm	1.1–50 µm
UBM Metallurgy (see footnote)																
RDL Conductor Thickness																
a. Standard Logic and Analog/Linear (low power)	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm
b. Standard Logic and Analog/Linear (high power)	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm	2–15 µm
RDL Metallurgy (see footnote)																
Wafer Saw Street Width minimum(µm)																
a. All saw based singulation for WLP	45 µm	45 µm	40 µm	40 µm	40 µm	35 µm	35 µm	35 µm	33 µm	33 µm	32 µm	32 µm	31 µm	31 µm	31 µm	31 µm
b. Advanced singulation (non saw techniques)	20 µm	20 µm	20 µm	15 µm	15 µm	15 µm	15 µm	15 µm	12 µm	12 µm	12 µm	12 µm	11 µm	11 µm	11 µm	11 µm
Package Pincount Maximµm																
a. WLCSP	240	256	256	256	289	289	289	300	300	300	300	300	300	300	300	300
b. Fanout WLP	550	600	650	650	650	700	700	700	700	700	700	700	700	700	700	700
Package Ball Pitch Minimum (Note 6)																
a. All WLP	250 µm	250 µm	250 µm	200 µm	200 µm	200 µm	200 µm	200 µm	175 µm	175 µm	175 µm	175 µm	150 µm	150 µm	150 µm	150 µm
Package Preformed Solderball Max Diameter for Min Ball Pitch (Note 6)																
All categories	100 µm	100 µm	100 µm	75 µm	75 µm	75 µm	75 µm	75 µm	65 µm	65 µm	65 µm	65 µm	55 µm	55 µm	55 µm	55 µm
Package Minimum Backgrind Thickness (Note 6)																
a. WLCSP	100 µm	100 µm	90 µm	90 µm	90 µm	90 µm	80 µm	80 µm	80 µm	80 µm	75 µm	75 µm	75 µm	75 µm	75 µm	75 µm
b. Fanout WLP	200 µm	200 µm	190 µm	190 µm	180 µm	180 µm	175 µm	175 µm	160 µm	160 µm	150 µm	150 µm	150 µm	150 µm	150 µm	150 µm
Type of WLP structure and metallurgy (bump, ball, column, solder, Cu, other) (see footnote)																
Multiple Die Wafer Level CSP (Max. dies)																
a. Memory (Stacked)	8	8	8	8	12	12	12	12	12	12	12	12	12	12	12	12
b. Standard Logic and Analog/Linear (Stacked)	3	3	3	3	3	3	3	3	4	4	4	4	4	4	4	4
c. Wireless: Bluetooth, FM, GPS, WIFI (Stacked)	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
d. Wafer level fanout (3D Stacked)	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
e. Wafer level fanout (2D Side by Side Die, each package)	6	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
f. Wafer level fanout (2D Side by Side Discrete Components, each package)	10	12	14	16	16	16	16	16	16	16	16	16	16	16	16	16
Stacked Die Wafer Level CSP Interconnect method (Through silicon vias, face to face, others)																
a. Memory	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias
b. Standard Logic and Analog/Linear	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias	Mix of wire bond and flip chip stacked dies. Through Silicon Vias
c. Wireless: Bluetooth, FM, GPS, WIFI	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias	Through Silicon Vias
Fanout WLP Technology	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules	Single Die 2D Multi Die Passives Through Vias, Doubled-sided Modules

Notes for Table 4



Notes

1. Entries defining the metallurgy that do not show changes over the next 15 years have been removed from the table. Any changes that might occur will be a result of the development of new materials.
2. the definition of WL-CSP is limited to 1.2 times die dimension or 1.4 times die area. Otherwise the fan out product would be just fan out WLP vs. CSP
3. Ball Mettallurgy is projected to be SAC for the next 15 years
4. UBM Metallurgy will have a number of variations depending on the company and the specific application. The metallurgy is not projected to change over the 15 years of the Roadmap.
5. RLD Metallurgy will have the same metallurgy for all device types and it is not forecast to change over the 15 years of the Roadmap
6. Type of WLP structure and metallurgy (bump, ball, column, solder, Cu, other). This metallurgy is not projected to change over the 15 years of the Roadmap. The metallurgy will be 2ML/2P/ Plated Cu/Solder Bump/Ball/ Copper Pillar where ML= metal layer and P=polymer.
7. These parameters are driven by PCB manufacturing and cost issues and do not represent a limitation of the technology.

PANEL PROCESSING

The logical next step is to expand FOWLP to higher levels of parallelism through panel processing. Figure 15 below illustrates the path to increasing parallelism in packaging for cost reduction, which has been underway for many years.

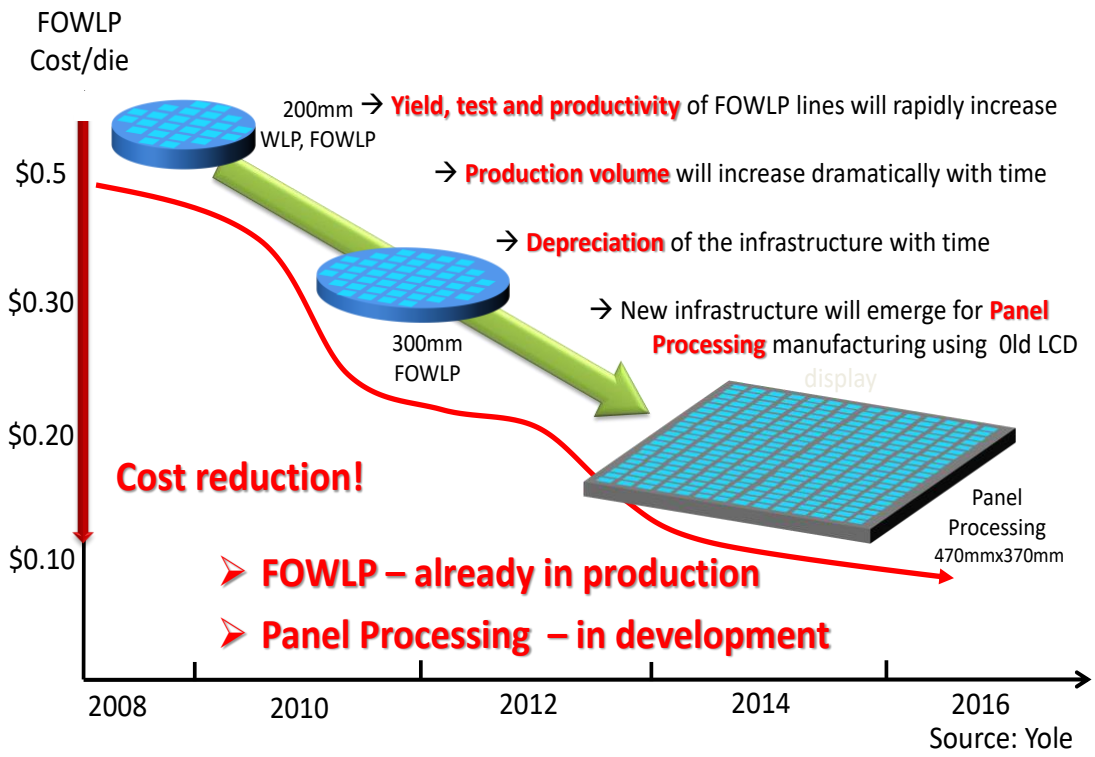


Figure 15: Cost reduction through increased parallelism in packaging.

There are difficult challenges associated with implementation of panel processing while maintaining all the advantages of WLP outlined above. These challenges include:

- Panel warpage (for Assembly accuracy & Manufacturability)
- Heterogeneous materials and non-symmetric structure causing bow
- New Polymer materials with matched CTE & modulus and low shrinkage needed
- Optimized layer sequence and design required
- Accuracy/Resolution
- Improved optical recognition systems for placement equipment
- Die shift compensation
- Imaging with high depth of focus and high resolution
- Local alignment - LDI or scanner or stepper
- Yield (and thus Cost)
- Suited materials and components
- Optimized processes
- Production experience
- Low κ dielectrics for RDL to support high speed circuits
- Low κ with low loss are essential for RF performance

The use of Panel level processing is just being introduced into manufacturing and the typical process flow is illustrated in Figure 16 below.

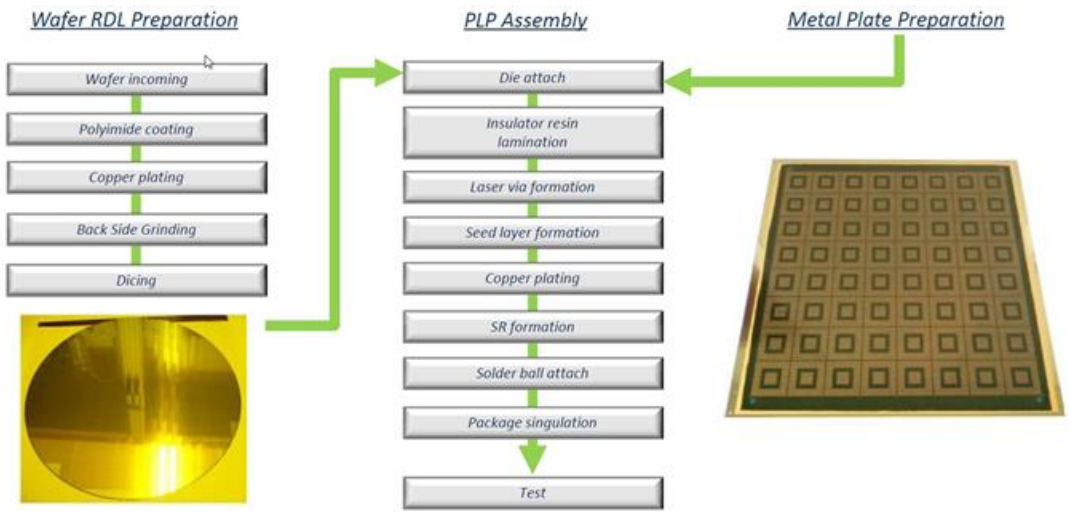


Figure 16: Panel level process for RF device (source: A Katsumata, Semicon Taiwan, 2015).

TECHNOLOGY NEEDS

PRIORITIZED RESEARCH NEEDS (> 5 YEARS RESULT)

Many of the challenges coming in the next 15 years of photonic packaging, both for single devices and for heterogeneous integration with other system components in 3D SiP products, are complex and will require years of R&D to identify, develop and move to low cost production. Some of the critical research needs are listed in the Table 8 below.

Table 8: Critical Research and Development Needs.

Critical Research and Development Needs
• New materials with low temperature processing for packaging electronic/photonic circuits • Low CTE conductors with improved electrical conductivity • High κ dielectrics with high fracture toughness and interfacial adhesion • Low κ dielectrics with high fracture toughness and interfacial adhesion • Substrate materials CTE matched with components • Thermal conducting material for heat spreading and heat sinking much better than Cu • Encapsulant materials with low CTE and low modulus to avoid transmitting stress
• New processes for joining stacked die at low temperature and minimum layer thickness
• Zero residue adhesive to facilitate low cost high quality wafer thinning
• Design & simulation tools for 3D heterogeneous electronic/photonic integration • Including materials properties for composites and very thin layers • Capable of design verification and optimization in the computer without need to fabricate prototypes • Co-design of thermal, electrical, optical and mechanical properties
• Standardize platforms and parts • Receiver • Transmitter • Transceiver • Multiple optical I/O need to be standardized for each family
• Optical connections to the package and perhaps on package that support
• Single mode WDW data into and out of the package • Low cost to manufacture • Alignment that is adequate for the purpose (perhaps with expanded beam) • Equipment for assembly of optical connections at high speed and low cost

PRIORITIZED DEVELOPMENT & IMPLEMENTATION NEEDS (< 5 YEARS RESULT)

The top-level difficult challenges will be the reduction of power per function, cost per function and latency while continuing the improvements in performance, physical density, reliability and security. Historically scaling of transistors has been the primary contributor to meeting required system level improvements but this scaling is reaching its limits. Moving photonics closer to the transistors and heterogeneous integration can provide solutions compensating for the shortfall from the historical pace of progress we have enjoyed from scaling CMOS.

Packaging and testing have found it difficult to scale their performance or cost per function to keep pace with transistors and many difficult challenges must be met to increase the rate of progress in packaging to maintain the historical pace of progress for data-based industry. The key elements of the IPSR-I packaging chapter are illustrated in Figure 17.

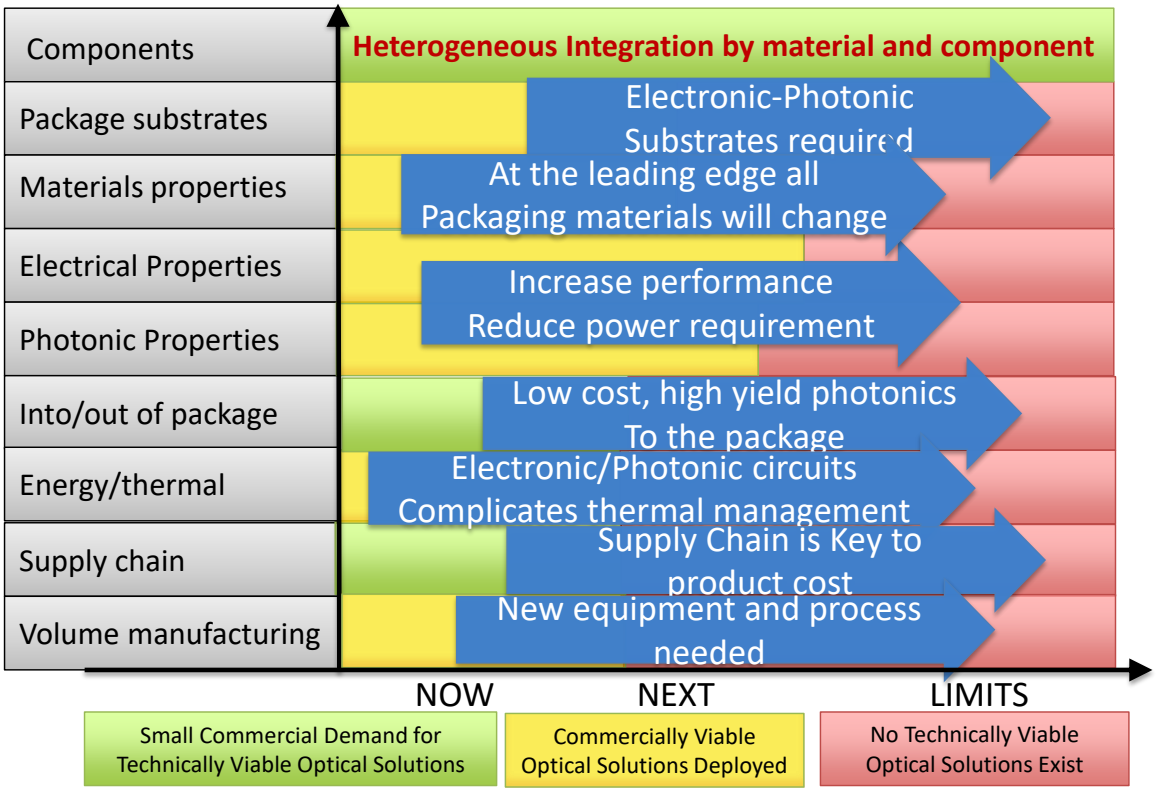


Figure 17: Photonic System Packaging Roadmap.

The elements in yellow have known technical solution that do not meet the full requirements, with cost and power being the primary reasons for shortfall. The elements in red currently have no known technical solution. Both categories pose difficult challenges.

So, challenges can be grouped in to three categories: (1) On-chip interconnect, (2) Package assembly and (3) Test. These are analyzed to define the challenges that have the potential to be "show stoppers" for the application areas identified above.

On-Chip Interconnect Challenges

The continued decrease in feature size, increase in transistor count and expansion into 3D structures are presenting many difficult challenges. While challenges in continuous scaling are not addressed here, the difficult challenges of interconnect technology in devices with 3D structures are listed. The challenges of incorporating photonics on a non-photonic chip versus the benefits of doing so are not yet clear. It is most likely that on-chip interconnect will be all electronic due to cost, switching speed and reducing interconnect length benefits associated with 3D-TSV architectures. The challenges addressed here assume that there is no optical interconnect on non-photonic chips. If innovation allows on-chip photonics (other than photonics chips) to be advantageous there will additional challenges not addressed here.

Package Assembly Challenges

Package assembly is often the limiting factor in performance, size, latency, power and cost. Although much progress has been made with the introduction of new packaging architectures and processes through innovations in wafer level packaging and system in package for example, a significantly higher rate of progress is required. The complexity of the challenge is increasing due to unique demands of heterogeneous integration of electronic/photonic circuits. This includes integration of diverse materials and diverse circuit fabric types into a single SiP architecture and the use of the 3rd dimension. Many of the problems are the same as those addressed in the on-chip difficult challenges section. The additional difficult challenges associated with the package are listed below.

TSV Formation [Cost: Design, Process, Materials] Aspect ratio (via last) drives cost higher and the differential CTE causes local stress.

TSV Operation [Reliability: Design, Materials] "Cu pumping" out of the vias on thermal cycling. Thinner layers and reduced CTE differential will be needed.

TSV Keep out area [Design, Materials, Process] Circuit density and cost are impacted large keep out area due to differential CTE and increased stress sensitivity for photonic components. New materials and lower processing temperature are needed.

Physical Density of Bandwidth [Size, Bandwidth: Design, Process, Materials] Single mode WDM replacing multi-mode fiber/wave guides and integrated photonics chip supporting this capability on-package are needed.

Low cost reliable optical connection to the package [Design, Materials equipment and Processes] Process, materials and equipment for alignment/placement, bonding process for "wave guide soldering" to make cost effective and reliable connections to the package are needed.

Low Cost Electronic/Photonic Package Substrate [Bandwidth, Waveguides, Design, Process, Materials] Mechanical stability, thermal management, warpage control, photonic connections, electrical connections, integrated passive devices and other components will need to be accommodated. There are many candidates for package substrate material that satisfy some of the requirements including glass, silicon, organic and ceramic but none of them satisfy all requirements. Silicon has the advantages of good CTE match, high electrical bandwidth, compatibility with optical waveguides and the wealth of experience, equipment and process technology from silicon IC fabrication that can be cost effectively reused. Glass has many electrical advantages but has poor thermal conductivity. Organics lack mechanical stability. Ceramics are expensive and also have thermal management limitations. It is likely that more than one of these substrates will be used for different applications.

Thinned Wafers/Die at Low Cost [Design, Equipment, Materials, Process] Today thinned die are typically processed to 50 µm thickness and at that thickness will be warped to a level that they cannot be stacked without a method for maintaining flatness. Low cost residue adhesive and equipment to use it effectively in the thinning process will be required. Wafers in production will be thinned to 20 µm thickness and lower during the life of this Roadmap. Techniques that work are known today but are not cost effective.

3D Stacking [Cost, Process, Bonding, Thermal Management] The processes used today are complex can be simplified with some expensive steps removed to lower cost and improve reliability. New materials and designs will be required for thermal management. Low temperature processing will be required.

Stacking Heterogeneous Components [Design, materials, process] There may be applications where the lowest cost and highest performance will require stacking of Si circuits and compound semiconductor circuits in the same stack. Differences in stress sensitivity and mechanical/thermal properties. New designs and materials will be needed.

Noise and Cross Talk in SiP [Design, Process, Materials] The SiP products will contain RF and other components that have low energy signals and logic that can draw high currents and impact the delivered power. Similarly, as we reduce the physical separation of components in 3 dimensions cross talk can prevent proper operation. Some of these problems will become increasingly difficult as we reduce operating voltage due to both smaller geometries and the desire to reduce CV^2 energy requirements of the package. Designs that use optical signals where practical and shielding where optics is not practical will be required. New materials and processes will be required to manufacture these elements at low cost.

Package Test Challenges

Known Good Die [Design, Test Contacts, Materials, Process, Equipment] The packaging of multiple die in the same package has relied upon *known good die* to ensure yield after assembly. This will not ensure reliability when transistors wear out and Very Large Scale Integration ICs today do not produce known good die. When there are billions of transistors per IC and the geometries are measured in nano-meters all die will have some defects. Intelligently designed redundancy can ensure a high yield of functioning die as they have in memory circuits for years. The concepts and implementation of testing to ensure functioning die for logic is still a work in process. Contactless methods for test point access are being investigated but are not yet practical.

Testing Silicon Photonics Chips at Wafer/Panel Level [Design, Equipment, Materials] Low cost production of Integrated Photonics will require manufacturing and testing of packages with a high degree of parallelism. Wafer level packaging will require testing at wafer level to maintain cost. The design of low-cost test solutions for single mode WDM photonics will be required. These solutions will be dependent on the co-design of the PIC, the test point contact and the test equipment itself.

Low Cost Optical Test Access [Design, Materials, Process] The incorporation of WDM single mode photonic signals on a package will require the ability to test the connections after package assembly. New concepts are under consideration, but a cost-effective solution does not exist. There will be design, materials and process changes to provide solutions.

3D Stacking [Design, Testing, Testing Access Process, Equipment] Testing and test access will require new designs for test access of stacked components. New test equipment to cost effectively test logic, memory, analog component, RF and passive devices in a single package will be required.

Test Contactors for Contact Pads Below 5 Microns Diameter [New Contact Methods, New Materials, Design] The test contactors in use today for electronics damage the pads they contact. This problem will be exacerbated as test pads are driven to thinner metal and sub-micron geometries. New test methods, new contact methods and new access design will be required, all must be low cost.

SiP Reliability [Design, Testing, Thermal Management] The more difficult challenges are associated with testing in a world where transistors wear out. We will have no known good die, traditional test access points will not exist and thermal management when areal thermal density is increased by a multiple determined by the number of layers in a stack will all require solutions. Innovation in design, materials and test strategy will be required to meet these challenges. New processes and materials will be needed with built in self-test, continuous test while running, intelligent redundancy and dynamic self-repair will be part of the solution. New materials and modifications to equipment will be required.

Ensuring System Reliability for Electronic/Photonic SiP based Systems [Design, Software, Fault Localization] The potential for a single point fault to prevent operation of data communication and analysis systems does not meet market requirements. There are two paths to reduce this probability of a system level shut down due to a single point failure. One is the use of intelligent redundancy which is identified above. The second is a system capable of quickly obtaining the physical location of a fault during the product qualification process so that revisions can be made to the design to remove or reduce the weak points in the system. The design of such capability for individual integrated circuits has been explored for several years. Extending this capability to cover all components in a complex 3D Heterogeneous SiP is a very large task but will become a requirement to contain the cost of excess redundancy in these systems.

Enabling the Software Defined Networks (SDN) with Real Time Testing [Design, Software] The diverse needs of users connected to the global network for access to the cloud will require SDN capability. This will not be practical unless the network hardware and software are configured to enable SDNs. This enablement will require low latency switching to set up the network and test capability to ensure that it is functioning correctly when set up and reliable during operation. The test challenge will require test resources at various points in the network that involve SiP incorporating FPGA technology.

Packaging Challenges by Circuit Fabric

Logic: Hot spot locations not predictable, high thermal density, high frequency, unpredictable work load, limited by data bandwidth and data bottle-necks. High bandwidth data access will require new solutions to physical density of bandwidth.

Memory: Thermal density depends on memory type and thermal density differences drive changes in package architecture and materials, thinned device fault models, test & redundancy repair techniques. Packaging must support low latency, high bandwidth large (>1Tb) memory in a hierarchical architecture in a single package and/or SiP). Memory will have multiple circuit fabric types for various applications and each will have differences in packaging challenges.

MEMS: There is a virtually unlimited set of requirements; hermetic, non-hermetic, variable functional density, plumbing, stress control, and cost-effective test solutions.

Photonics: Extreme sensitivity to thermal changes, O to E and E to O, Optical signal connections, new materials, new assembly techniques, new alignment and test techniques

Plasmonics: Requirements are yet to be determined but they will be different from other circuit types

Micro-fluidics: Sealing, thermal management and flow control must be incorporated into the package.

Most if not all of these will require new materials, new processes and new equipment for package assembly and test to meet the 15 years Roadmap requirements for electronic/photonic systems.

Packaging Challenges by Material

1. **Semiconductors:** Today the vast majority of semiconductor components are silicon based. In the future both organic and compound semiconductors will be used with a variety of thermal, mechanical and electrical properties; each with unique mechanical, thermal and electrical packaging requirements. Photonics and power management ICs will incorporate compound semiconductors with different thermal and mechanical properties.

2. **Conductors:** Cu has replaced Au and Al in many applications but this is not good enough for future needs. Metal matrix composites and 2D ballistic conductors will be required. Inserting some of these new materials will involve new assembly, contacting and joining techniques.

3. **Dielectrics:** New high k dielectrics and low k dielectrics will be required. Fracture toughness and interfacial adhesion will be the key parameters. Packaging must provide protection for these fragile materials.

4. **Molding compound:** Improved thermal conductivity, thinner layers and lower CTE are key requirements.

5. **Adhesives:** Die attach materials, flexible conductors and residue free adhesives needed do not exist today.

6. **Underfills:** Needs to flow under the chip and bond it for the long term stability is challenge.

GAPS AND SHOWSTOPPERS

The gaps between requirements and the technology available are listed in Tables 9 and 10 below. These tables are coded according to priority. High priority gaps are those likely to become showstoppers during the 15 years covered by the Roadmap. Lower priorities are important but have known alternatives that can be used until development closes the gap.

They are also coded by category. You will find the definition of the coding abbreviations at the bottom of Table 10.

Table 9: Gaps and showstoppers < 5 Years.

Priority	< 5 Years (Tactical) Gaps/Needs	Category	Comments:
H	Creating a roadmap that covers the emergence of "more than Moore" packaging integration (System in Package, MEMS, sensors, analog centric technologies, opto electronics, heterogeneous integration including all of the above, etc.)	R/S/O	Electronic roadmaps have been driven by primarily by CMOS logic and memory. The emergence of System in Package, MEMS, photonics, sensors, RF, power devices, heterogeneous integration, etc. are not yet fully supported. Treatment of packaging needs for these new technologies must be addressed to identify research and development requirements.
H	Molding Compounds with better properties and lower cost.		Need something with H2O uptake <0.1%, that adheres to leadframes and dielectics with κ less than 3.0, TCE of ~15ppm/degree C., costs less that $10Kg, "molds" at <100C, has an oxygen burn index >25%, contains no Cl or Br and will tolerate post molding temperatures of 250C.
H	SiP components and systems reliability requirements drive the need for tools and procedures that are not yet available. Test access will be a limiting factor for SiP and new approaches will be needed.	R/S/O	Failure classification standards, failure mechanisms, analysis techniques and methods, electrical, thermal and mechanical simulation and co-design, lifetime models with acceleration factors, and test vehicles for reliability characterization are needed.
H	Better understanding of interfacial science of adhesion / delamination of packaging materials and interfaces in use today is needed. This area is one of the key areas that will impact future yield and reliability.	R	This is a major issue that packaging engineers deal with daily. It is more critical for thin die and Cu/low k interconnect. Research is required on chemical and mechanical interfacial science of adhesion and delamination that allow design of systems that will not delaminate.
H	There is no clear consensus regarding the preferred flip chip interconnect method for FCCSP/FCPOP products in 22nm node and beyond. Standardization to drive economies of scale and industry infrastructure development are needed.	S/O	The use of solder plated bumps, Cu pillar, Au stud, area array and/or perimeter bump patterns, lines and spaces, via pitch design rules, etc. are addressed in this Roadmap but optimization and standards are required to meet the cost/performance targets.
H	Flip chip packaging with tighter pitch, lower processing temperature and reduced cost are needed to complement the performance and other advantages of flip chip technology for packaging.	R/O	Low cost and high reliability for large, thin die flip chip will require additional research and optimization.
H	There is a need to increase R&D investment to accelerate progress in under fill technology. New disruptive technology / out of the box thinking is required as the pitch shrinks and die size increased.	R	New materials will be required. Potential solutions include pre-applied under fill materials that can support reflow of 50um and smaller interconnect pitches; non-capillary under fills for 30um or less in line flip chip for FC-CSP / FC POP products; Designs that do not require underfill should be explored.
H	Need lower cost multi layer RDL interposers (silicon, organic or glass)	R/O	Existing technologies are very critical and work but they are not cost effective today, need step function cost reduction
H	Package warpage at elevated temperature (SMT, reflow) will drive the need for new materials, new package architecture and new low temperature assembly and packaging processes.	R/O	Warpage is becoming the primary limiting factor to support large area die and interposers. It limits ball pitch, ball size in BGA packages,interposers and TSV Package on Package SMT.
H	Need for optimized, lower cost of ownership and high throughput equipment for wafer level packaging, fanout, 3D and interposer assembly and System in Package	O	Current equipment is mostly modified wafer fab equipment or equipment designed for single die packaging not cost effective nor designed or optimized for wafer level packaging or multi-die SiP processes.
H	wafer thinning and packaging of thin die will require new, cost effective equipment, materials and processes.	R/O/S	This issue becomes more critical as wafer diameter increases and die thickness decreases, issues include stress relief, surface thickness variation, wafer warpage, handling after thinning, singulation, packing/shipment methods from wafer fabs to packaging houses.
H	Low cost photonic connection to the package that supports single mode fiber and WDM.	R/O	Physical density of bandwidth into and out of the package requires sinble mode WDM and smaller core makes alignment slow and therefore expensive. Driving down power is aided by moving photons as close to transistors as possible to reduce high speed electrical interconnects.
H	Need new high thermal conductivity materials for high thermal density devices	R/O	The new materials properties required have been included in the Emerging Research Materials Chapter.

Table 10: Gaps and showstoppers > 5 Years.

Priority	> 5 Years (Strategic) Gaps/Needs	Category	Comments:
H	Clear identification of packaging technologies needed to help close the gap in scaling until new technologies are availale to replace CMOS.	D/M/S	Packaging technology will partially close the gap while research institutions complete the R&D for new device technologies in order to continue to scale beyond CMOS.
H	There is a need to increase R&D investment in packaging technology and to increase the effectiveness of that investment to meet the challenges defined in the Roadmap.	D/M/S	Collaboration among researchers is vital to maximize the efficiency of investment. Universities and Research Consortia focused on Industry Packaging R&D and improvement in new technology commercialization must involve supply chain partners in R&D phase to improve technology transfer methods.
H	Package substrates remains the most expensive component in advanced packages. The trend is not improving but instead is going in the other direction. There is a need for innovations and potentially for new disruptive technologies to help to reverse this trend. This is the primary cost limiting factor for packaging.	D/M/S	Scaling in packaging costs must be closer to IC scaling to support continued price elastic growth of electronics. The limits of today's organic substrate technology will cannot be extended to meet this need. New materials and new processes will be required.
H	Medical electronics packaging will require materials and processes, that are bio-compatible, RoHS compliant and compatible with MRI systems	M	Medical electronics is an emerging growth opportunity in our industry that will drive the need for new materials and innovative packaging methods. Innovative methods to supply power, ensure greater reliability and reach greater levels of miniaturization are needed.
H	Some photonic active components are much too large (mach zender modulators) at >5µm and greater; others are too sensitive to temperator change (ring oscillator modulators).	D/M/S	Large components and very tight operating temperature range are very expensive and, in many cases, may decrease reliability. New materials and devices such as plasmonic devices may be a potential solution.
H	Improved design systems providing electrical, thermal and mechanical co-design and simulation tools that can be used as predictors of package/system reliability with high level of confidence will be a key enabler to meet the packaging requirements of the future.	D/S	The support of Research Institutes, Academia and EDA tool suppliers is critical to closet this strategic gap. The industry needs to identify all gaps and limitations of current modeling and simulation tools to help Universities and EDA tool vendors focus their research efforts. In addition, a materials properties data base covering all levels from the IC to the system board will be needed to apply the simulation tools.
M	Future generation of packaging technology will incorporate a wide range of new materials and equipment with capabilities not availabe today. These materials will include dielectrics with both higher and lower dielectric constants, vastly improved electrical and thermal conductivity and improved mechanical properties. We have yet to address the issues of new processes, new equipment and new safety issues required to incorporate these new materials.	D/M/S	When existing interconnect and encapsulation methods run out of steam and are replaced by different methods and materials what will the requirements for new equipment and processes be? An early start to develop answers to these questions will be necessary if we expect to have a timely and efficient incorporation of these technologies in future generations of packaging solutions and and efficient transfer from the developing the companies in the supply chain.
	Category for < 5 years (Tactical Gaps)		**Category for > 5 year (Strategic) Gaps**
H= high	Standards = S		Design = D
M=Med	Optimization = O		Energy & Environment = E
	Research = R		Manufacturing = Mfg
	Other = NA		Materials = M; System Integration = S

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CONTRIBUTORS

Peter O'Brien, Tyndall National Institute – Chair
Bill Bottoms, 3MTS – Chair
Tom Brown, Rochester University
David Mackey, mBryonics
Jeroen Duis, PHIX
Dick Otte, Promex
Sylwester Latkowski, Technical University of Eindhoven