ASSEMBLY

Contents

Tables

EXECUTIVE SUMMARY

Introduction: This chapter primarily addresses optical related assembly issues beginning with parts and wafers from a fab until the assembled device is ready for final test.

Assembly is the process of bringing together parts, aligning them accurately with respect to one another and then joining them permanently utilizing a variety of processes. Photonic devices have added, unique assembly requirements (fiber attach, submicron accuracy, Z axis assembly, particle elimination, etc.) compared to typical microelectronic and optical products. These issues are the focus of this chapter.

Many of the important applications require single mode technology where assembly of parts, especially fiber attach, requires submicron tolerances and stability of the optical chains over the lifetime of the product in the operating environment. Achieving that level of mechanical consistency requires starting with the design, selecting materials and structures to minimize the effect of temperature and stress and other environmental phenomena, selecting materials, joining methods, and assembly processes that will yield that result. Generally, materials with high modulus (E) and low Temperatur Coefficient of E (TCE) are best and have been used extensively in optical devices. Unfortunately, these materials tend to be expensive so much effort is devoted to utilizing lower cost materials and the lower cost processes.

Substantial overall cost reduction of optical devices is required to make optical products economically viable in more applications. Since packaging and assembly is a large fraction of the cost of current devices, the focus of this chapter is on reducing these costs.

Current Status: An obvious way to avoid assembly cost is to minimize the number of parts to be assembled. That is being addressed through the increased use of integration at the platform level in the front end. Unfortunately, all of the functions needed in optical applications cannot be integrated yet so parts made with appropriate technologies are combined in what is now called heterogeneous integration. Assembling this complex mix of parts is heterogeneous assembly.

Assembly needs are strongly influenced by the trend to make optical devices smaller, meaning device measured in mm vs cm. Also, the inclusion of single mode components requires submicron bond line thickness control in joints and location tolerances. These tolerances are going from mils in electronic assemblies to microns and submicrons in single mode devices. In addition, sensors incorporate not only Photonic Integrated Circuits (PICs) but other specialized parts that impose constraints on the assembly process and restrict and limit assembly options. Many optical devices incorporate fragile, environmentally sensitive parts including InP parts, polymer based devices, SiN, GaAs and GaN substrates and components that impose further assembly limitations. Finally, optical devices are often three dimensional rather than planar. The net result of these unique more demanding requirements is that new joining methods utilizing new materials and process equipment are needed.

Main Challenge: The main challenge is cost reduction of optical devices to make optical products economically viable in more applications. A challenge to developing capabilities to reduce cost is the relatively small volume (tens of thousands vs. millions) of photonic devices that are built compared to electronic devices. The potential revenue from the sale of these processes is often not great enough to recover their development costs. A current important challenge is reducing the cost of submicron fiber and fiber array alignment.

Another challenge is developing methods to eliminate optical fiber pigtails. Their inclusion makes manufacturing difficult and expensive. Alternatives such as waveguides built into substrates and circuit boards are emerging as an alternate solution. This will require joints and the related assembly processes between parts and waveguides on substrates and in boards.

Developing a robust supply chain for parts with needed characteristics such as fiducials, tight tolerances, smooth, straight flat edges, good plainarity, consistent lot-to-lot properties, etc. for optical products is a challenge.

Needs: The overall cost, including the cost for assembly, of optical devices needs to be reduced substantially to make optical products cost effective in more applications. The recent growth of data center applications is driving an unprecedented high level of demand for photonic devices. The data center era demands fast-paced innovations and concurrent manufacturing of multiple generations of photonic devices through volume production.

This increasing volume with the high mix nature of photonic manufacturing calls for a new generation of assembly processes that is enabled by new equipment that is easy to tool and program for a new application, easy to setup for a repeat job, with high flexibility and with high (submicron) precision. This is a very different set of requirements from that of conventional semiconductor production equipment where equipment is typically configured for a specific application and rarely changed. This electronic equipment is not optimum for photonic applications because the cost of frequent change-over is high in the high mix low volume environment typical of photonic devices.

Another need is for the detailed mechanical and optical properties of the materials used in optical products that are often not available. Standardizing on those materials and making the properties available will enable designers to model optical products better and minimize the need to build and test hardware.

Finally standards are needed to minimize development efforts and enable solutions, once developed, to be used in many devices. As with other industries, standards will emerge as volume grows, new devices are introduced and incorporate parts and processes that are available.

Table 1. Assembly Challenges in Future Years

2024	2029	2034
Low cost active alignment for fiber arrays and edge emitters	Developing methods to build optical functions in the Z direction with submicron accuracy and optical quality surfaces.	Submicron alignment of optical beams to metamaterials to enable the materials to perform highly specific functions.
Assembling 128 fiber linear arrays to PICs with < 0.5 dB loss/fiber for < $0.10/fiber	Designing three dimensional optical devices utilizing software that incorporates mechanical, electrical and thermal requirements	Achieving 0.01 micron dimensional tolerances to implement new functions
Developing supply chains for high tolerance parts; clean edges, tight dimensional control, lot to lot repeatability, etc.	Implementing methods to optically connect large fiber bundles (64 x 64 = 4096 fiber) to PICs.	A production method of fabricating optical waveguides in-situ to transmit light with low loss from a source to a sink. i.e. optical “wire bonding”
Developing die attach methods that provide submicron thickness tolerances	Developing an optical electronic platform that will serve many applications with minimal customization	Developing assembly methods to enable wavelength selection to 1 part in 10^6 and extracting signals that are 60+ dB lower in strength than overlapping signals.
Developing supply chains for materials with repeatable joining dimensions, especially organic compounds with fillers with minimal lot-to-lot variation.	Developing methods that join parts without the addition of joining materials such as epoxy or solder to minimize variation in final dimensions by eliminating bond line variation.	Developing assembly tools that have nanometer resolution.
Developing methods to protect InP and other water and oxygen sensitive materials, surfaces and		

components from the environment		

These Challenges assume:

1. The cost for optical functions decreases > 10%/yr.
2. Optical devices become smaller limited only by optical wavelengths.
3. Tolerances required become far smaller than the wavelength of light.
4. The most challenging requirements result from single mode and low level optical signals.
5. Data Communication rates continue growing, meaning per lane and through the internet.
6. Meta Materials arise as an enabler.
7. Non-linear optical phenomena come into use to provide additional functions.
8. 3D printing of single mode optical devices and optical quality surfaces becomes viable.
9. Monolithic integration capability grows to enable inclusion of direct bandgap materials.
10. PICs are monolithically integrated with electronic functions.
11. The number of optical devices built and sold grows at ~ 25%/yr.

PRESCRIPTIVE ASSEMBLY RECOMMENDATION

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS

Passive alignment (chip-to-chip, die-to-die, and fiber-to-chip, fiber-to-die):
We will need some designs/devices that will relax the tolerance for the passive alignment to small waveguides. Preferably, these structures (tapers or spot size/mode field converters) need to be transferred to the front end so that they are included in the fabrication of the chips.

Of course, these structures should pass all the reliability tests (are robust) and these functional building blocks should become available between now and 5 years, since interface losses are the main limitation in the total link budget.

What would be the maximum relaxation of the tolerances that can be achieved?
That will determine the development of equipment that can do the assembly in an automatic manner (in 10 years) within that tolerance. Meanwhile (5 years), there could be semi-automatic equipment. This is for coupling from chip-to-chip and from fiber-to-chip.

Active alignment, strategy and implementation requirements:
For active alignment, typically we will need a shunt waveguide connecting one side of the chip to the other one. Like this the fiber arrays can be actively aligned, using the outermost fibers for active alignment. In devices where the input and output should be in different sides of the chip (or to take advantage of the whole periphery of the chip) other types of devices for alignment are necessary:

- Structures for wafer-level testing of devices prior to assembly.
- Standard packaging flows to be compatible with the developed equipment (5 -10 year). Working together with the equipment developers.
- 3D packaging/stacking of different dies with different materials and functionalities: through bias? Heat management? Materials to bond the dies?
- Photonic interposers? And interfaces with the different chips in different technologies?

Degree of integration: The greater the amount of parallel processing usable in fabrication, the lower the cost.

Number of parts: Minimizing the number of parts that need to be purchase, shipped in, inspected, inventoried, issued to manufacturing, assembled, tested and inspected reduces the cost of products.

Cycle time for an assembly: The second most important cost driver is the amount of time needed to build a device. This is the time which equipment or individuals apply to each device; waiting time in queues is excluded. Each step is typically assigned a $/minute that is charged to a device along with the part costs and overhead rates (usually a percentage of the prior costs) to establish the total cost.

Joining time: A key contributor to the assembly time is the time to form joints. Solders, for example, must cool, epoxies cure to at least a B- stage, welds must cool, etc. Minimizing these times minimizes cost.

Optical chain movement over time: Many single mode devices, that are expected to dominate optical devices in the long run, require stability of location over the lifetime of the product of 0.1 microns.

Part presentation: Minimizing assembly time requires minimizing the time needed to handle and feed parts to the assembly processes, especially machinery. Shipping parts as sawn wafers on tape or die attach film, in tape and reel, in trays, in waffle pack, or other standard method minimizes handling, losses and damage, all of which reduce cost.

Handling fibers, either singly or as arrays, in automatic machinery is difficult, especially if the fibers are lengthy, meaning more than a few centimeters.

Test time: Testing is often expensive, especially design verification and the engineering of software and fixtures for in process and final testing. Long test cycles can raise cost rapidly if expensive test sets are needed.

Several presentations and listing of the key attributes have been developed and proposed. Below is a compilation of those listed:

Table 2. Roadmap of Quantified Key Attribute Needs	[unit]	2020	2025	2030	2035	2040
Single Mode (SM) fiber attach to substrate	sec/joint	300	133	44	25	15
SM optic component placement to <0.5 micron accuracy without fiber	sec/part	30	15	10	7	5
Multi-Mode (MM) part placement to <5.0 micron accuracy	sec/part	5	3	2	1.5	1
Wafer sizes (InP / GaAs / Si)	inch	3" / 6" / 12"	4" / 6" / 12"	4" / 8" / 12"	6" / 12" / 18"	6" / 12" / 18"
Max Die sizes (InP / GaAs / Si)	mm^2	10x10 / 10x10 / 75x75	12x12 / 12x12 / 75x75	12x12 / 12x12 / 75x75	15x15 / 15x15 / 75x75	15x15 / 15x15 / 75x75
Min Die sizes (InP / GaAs / Si)	mm^2	0.05x0.05 / 0.05x0.05 / 0.05x0.05	0.05x0.05 / 0.05x0.05 / 0.05x0.05	0.05x0.05 / 0.05x0.05 / 0.05x0.05	0.05x0.05 / 0.05x0.05 / 0.05x0.05	0.05x0.05 / 0.05x0.05 / 0.05x0.05
Die minimum thickness (InP / GaAs / Si)	microns	75 / 125 / 25	75 / 75 / 20	50 / 50 / 15	40 / 35 / 12	35 / 30 / 10
Chip-chip coupling loss type	N/A	Waveguide, free space optics, end-facet, grating	Waveguide, Free space optics, end-facet, grating	Photonic wire, Monolithic integrated	Monolithic integrated	Monolithic integrated
Chip-chip coupling loss	dB	< 1	< 0.5	< 0.2	< 0.2	< 0.2
Wafer dicing (InP / GaAs / Si)	process	Cleaving, laser dicing / cleaving, sawing / sawing, wet etching	Cleaving, laser dicing / cleaving, sawing / laser dicing, plasma etching	Cleaving, laser dicing / cleaving, sawing / laser dicing, plasma etching	Cleaving, laser dicing, sawing / cleaving, sawing / laser dicing, plasma etching	Cleaving, laser dicing, sawing / cleaving, sawing / laser dicing, plasma etching

Fiber array alignment	TBD	TBD				
Copper pillars, solder cap (pitch/dia.)	microns	100/50				
Through Substrate Vias (TSVs) pitch / size / accuracy	TBD	TBD				

CRITICAL (INFRASTRUCTURE) ISSUES

Key challenge for assembly of the PLCs / PICs to achieve low-loss coupling between:

- fiber-PIC
- laser (active/passive)-PIC
- PIC-PIC

Current strategies are based on direct coupling, or in the case of mode-mismatch, using a lens or a free space optics microbench as used by Kaiam/Broadex Technolgies.

Optically and fundamentally there are no challenges to achieve this except the accuracy required and the multi axis dependence of the interconnect loss that is difficult to achieve in a robust and durable assembly.

A practical issue is handling fiber, either singly or as array, especially if the fibers are more than a few cm long. The end of the fiber to be joined to another component can be held in various ways; the difficulty is the other cms of the fibers that tend to "flop" around and are hard to control without specific fixtures and handling equipment.

In case of applications with blue light and UV light (wavelengths less than 600 nm) one needs to pay particular attention to reliability since energy densities and optical power increase with decreasing wavelengths.

It is very clear that an infrastructure for active alignment is required:

- The changes during curing of epoxies or solder should be tracked real-time.
- Automation is the main challenge.
- The cost of die-bonders and alignment stages require (still) significant investment.
- For reliability and temperature cycling it is important to pay consideration to thermal coefficient of expansion-matching between various components.

In case micro-arms are used (not recommended) one needs to pay attention to vibration modes.

TECHNOLOGY NEEDS

Prioritized Research Needs (> 5 year)

Table 3. Prioritized Research Needs (> 5 years result)	Relative Priority
Process to build reliable light sources that can be modulated at 50 GHz+ compatible with CMOS	
Highly integrated devices to minimize part count and the need for assembly	
Assembly equipment customized specifically for specific optical requirements	
Ability to locate parts to submicron tolerances.	
Software methods to simulate manufacturing processes to enable more rational selection of materials, processes and equipment	
Methods to fabricate optical components with submicron tolerances at low cost.	
High tolerance substrates/platforms that optical components are assembled on, possibly made with 3D printing and laser finishing.	
Nano-materials with improved properties	
Meta materials to provide new functionality	
Integrate packaging into the device rather than putting an optical structure into a separate package	
Erasable grating to put optical probe points on a chip without impacting the performance after the chip is packaged.	
Structures to convert light to plasmons to reduce the size of high frequency detectors	
A small and mechanically robust, thermal stabilized, platform that incorporates Photonic, RF and DC connections up to 60 GHz (32 Ph, 10000 DC, 256 RF)	
Achieve low-loss (< 1dB) hybrid optical interconnects with chip-chip and fiber-chip coupling for visible and IR applications (400 nm - 2.5 micron)	
Achieve compact high contrast photonic chips with low-loss monolithic interconnects (SSC) with Mode Field Diameter matching through development of monolithic tapers and spot size converters for visible and IR applications (400 nm - 2.5 micron)	
Footprint reduction of on-chip-GSG-RF interfacing (on InP) through hybrid InP-TriPleX RF-interposer.	

Prioritized Development & Implementation Needs (< 5 years)

Table 4. Prioritized Development & Implementation Needs (< 5 years result)	Relative Priority
Minimize the number of parts and number of assembly steps	
Metal to metal, epoxy, or alternate joining methods that are fast and provide stable joints over the life of the product.	
Developing the properties of standard materials for use in design.	
Design software able to utilize Hooke's General Law over temperature to ensure designs will function over the life of the product.	
Self-alignment/passive alignment (must avoid active alignment and testing to go to high volume)	
Standardize transmission media for short distances - On chip waveguides - On circuit board waveguides - Connectors for and to the above - Mode converters to SM fiber - Test interfaces	
Standardize platforms and parts - Receiver - Transmitter - Transceiver - Multiple optical I/O need to be standardized for each family	
Improved machine interfaces to minimize programming and set-up time to reduce costs for short optical product runs.	
Develop a budgeting method for product development - More training of designers in design for manufacturing, test and cost	
Achieve < 1 dB interconnect losses for hybrid chip-chip coupling for large spectral range (100 nm for telecom & spectrometry)	Critical
Achieve < 0.5 dB interconnect losses for hybrid fiber-chip coupling for large spectral range (200 nm for telecom & spectrometry)	Critical
A small and mechanically robust, thermal stabilized, platform that incorporates photonic, RF and DC connections up to 30 GHz (32 Ph, 1000 DC, 64 RF)	Critical
InP-on-top-of-Triplex RF-and-optical interposer solution	Critical
Achieve high (monolithic) integration density with active and passive components through use of high-contrast monolithic/heterogeneous/hybrid low-loss platform	Desirable
Process compatibility (zero change strategy) with current 150 mm/8"/12" CMOS foundry manufacturing infrastructure to achieve scalability to high-volume low-cost manufacturing	Desirable

GAPS AND SHOWSTOPPERS

Optically and fundamentally there are no challenges to achieving low cost single mode optical components but the high accuracy (typical 100 nm) and multi axis dependence of the interconnect loss is a challenge for robust and durable assembly.

Table 5. Gaps and Showstoppers
Continual improvement in electrical transmission methods keeping electrical methods less expensive than optical solutions
High cost resulting from the difficulties of integrate/combining a suitable light source with CMOS electronics
Difficulty eliminating active alignment. Some do not see active alignment as a problem, but as the solution. In fact active alignment is being used successfully in where the assembly process is engineered for the specific part and fibers being assembled. What is lacking and needed is a generic, widely applicable method of doing active alignment and the subsequent joining that is eacily adopted to different parts sizes, fiber arrangements, etc.
High costs resulting from low production volume due to limited applications and lack of standard methods
Difficulty of handling part smaller than 150 microns square. Vacumn tools and other standard pick up methods need detailed engineering to handle such parts and in some cases those methods do not work.
Component attach processes, and joining methods generally, that cause micro motion such as creep with epoxy during the curing step
Speed of suitable assembly, test and other process equipment resulting in high costs.
Joining processes with long cure/joining/cooling cycles that raise cost
Inability to overcome the cost driving, rate limiting step/bottle neck of manufacturing/testing Such as the Duration of UV or thermal cure steps and the number of assembly steps? “Time is money”
Limits resulting from adopting existing equipment, materials and methods to optical assembly and test
Difficulties resulting from optical chains occupying the third dimension (Z) and the requirement to build in that dimension in addition to the XY planar dimension common for electronics that is frequently built on a plain.
Achieving low cost heterogeneous assembly of III-V parts with CMOS devices.
Fabricating optical transitions from one media or device to another that minimize loss and alignment cost
Limited availability of manufacturing simulation tools and software
Designing for Manufacturing and test:

- Maximizing output to reduce cost - Studying designs to trade off accuracy and speed
Inability to utilize materials or processes due to environmental related constraints (RoHS, REACH, WEEE, etc. TBD)

RECOMMENDATIONS ON POTENTIAL ALTERNATIVE TECHNOLOGIES

Assembly in Z direction is required, in contrast to conventional surface mount assembly technology utilizing pick and place and reflow soldering when the results are suitable for the application.

Table 6. Recommendations on Potential Alternative Technologies
Explore the use of 3D printing to build a suitable substrate/platform upon which optical components can be placed, affixed and assembled in 6 dimensions that have smooth surfaces meaning to less than 0.1 microns RMS roughness.
Review the history of platforms for passive assembly (silicon optical bench) that have well defined mechanical stops and associated methods to affix/weld/glue parts in place and classify their characteristics for highly accurate optical assembly.
Explore methods utilizing capillary actions to “pull” parts into place to effect passive alignment.
Utilize laser machining to do micro and nano cutting and shaping to make highly accurate parts to implement passive optical alignment.
Utilize laser processing to make optical waveguides in-situ to fabricate optical connections and optical structures.
Utilize plasmons to minimize size and maximize functionality
Afix micro optic lenses or other mode matching devices to the ends of fibers and fiber arrays as an alternate to “butt” coupling fiber to components.

APPENDIX A – ASSEMBLY TECHNOLOGY

INTRODUCTION

Assembly is the act of combining all of the photonic and other components together into a device. The 2020 Integrated Photonic Systems Roadmap – International (IPSR-I) emphasizes the importance of system design in relation to the assembly and packaging strategy.

The total cost of photonic products, including the cost for assembly, needs to be reduced substantially to make them cost effective in more applications. Conventional wisdom says 80% of the cost of a product is determined by the initial design.

The designer of a device should evaluate the impact of assembly, packaging and related issues to minimize cost. An obvious way to avoid assembly cost is to minimize the number of parts to be assembled. That is being addressed through monolithic integration which is integration at the wafer level and is being addressed by the Silicon Monolithic, Silicon Nitride, InP, and polymer chapters. Unfortunately, all of the functions needed in optical applications cannot yet be monolithically integrated so assembly, hybrid/heterogeneous integration, as it is often called, is needed. The Assembly Technical Working Group (TWG) addresses the resulting and related issues.

Whereas the Heterogeneous Integration Roadmap[1] (HIR), a separate but related roadmap, focusses on the hybrid component integration, the focus of this Roadmap chapter is on the assembly issues related to PICs and optical components, thus it addresses the key attributes and critical challenges to incorporate PICs to enable photonic functions, especially interconnect.

The assembly process starts with the pre-assembly steps, followed by the alignment and joining processes which sometimes include active alignment strategies.

Pre-assembly mainly relates to wafer preparation; processing of wafers after they leave the front end fabrication process but before assembly begins. Wafers require “back end” processing including: thinning, singulation and sometimes applying a Die Attach Film (DAF) or back side metallization.

The pre-assembly steps include evaluating:

- The required system performance should be evaluated against the impact of operational environmental conditions such as temperature, humidity, etc. and more.
- The design requirements and their tradeoffs with assembly strategies need to be evaluated to develop an assembly strategy to enable low-cost, high-performance manufacturing of optical products.
- The dimensional variations in the fabrication processes (front-end and back-end) and the impact on performance under operational conditions need to be evaluated during package design to determine the proper housing and materials to cope with temperature changes, stress, shocks and mechanical movements.
- Performing the backend processes such as wafer thinning for different materials such as silicon, GaAs and InP, borosilicate glass, sapphire, GaN, SiC, PZT, etc.

[1] The HIR is a Roadmap sponsored by the IEEE and widely supported by industry that addresses heterogeneous Integration in a broader sense than this Roadmap that concentrates on Photonics Integrated Circuits and Photonics.

- Substrate and wafer singulation using conventional sawing, stealth dicing, thermal ablation or plasma dicing or even dice-before-grind methods need to be evaluated and the lowest cost method that meets the requirements selected.
- The use of DAFs, put on the back of a wafer before singulation eliminates the sequential dispensing of die attach epoxy and provides better control over epoxy thickness, fillet shape, voiding and final dimensions as well as post cure die location.
- Finally selection of the assembly processes, including test, and their sequence to complete the build.

Alignment brings the components geometrically together with respect to one another, usually by machinery.

The common passive alignment processes are:

1. Capillary action that "floats" or "pulls" parts to a location. The surface mount process utilizes this method. Solder paste is first deposited on "pads" on a substrate. Parts are placed on the solder paste approximately where they will finally be located. Heating the structure melts the solder which flows to the edges of the wettable surfaces on the part and substrate also floats the parts. Capillary action forces move the part in X, Y, and Z to an equilibrium location dependent on the amount of solder and the location and size of the wettable surfaces. Some recent innovations utilize capillary action to pull parts such as lasers or detectors against a "stop" to precisely align them. When the solder cools and solidifies, the parts are locked in place.

   This process works with other solders and brazing metals and with some epoxies and other adhesives.
2. Machinery that locates parts with respect to one another utilizing cameras and software that image fiducials or other references on parts and place parts.
3. Mechanical stops or alignment points such as V-grooves, steps or other geometric shapes that part are placed against are combined with machines that places the parts.

Active alignment measures the quality of the optical connection by sending light through the joint and moving parts to maximize transmission. At that point the parts are "locked" in place by a joining method such as one of those described below.

Joining fixes parts in place utilizing processes such as:

1. Solidification of solders such as described in (1) above.
2. Metal deformation bonding such as:
   a. Thermosonic and ultrasonic bonding such as used in wire bonding
   b. Thermocompression bonding of die with 1000's of IO, often as pillars.
3. Curing of polymers such as:
   c. Epoxies cured with heat
   d. Acrylates cured with UV
4. Fusion such as:
   e. Welding usually meaning the melting of metals
   f. Melting and solidification of glass, often as a frit.

Some level of description of the different assembly processes for photonic components is provided, including these topics:

- Conventional surface mount assembly technology

- High accuracy placement
- Joining equipment
- Flip-chip assembly
- Micro-Ball Grid Array (BGA)/Chip-scale self-alignment assembly
- Wire bonding
- Dispensing of organic adhesives, encapsulants and underfills
- Joining with UV cured adhesives
- Assembly in a particle free environment

Of particular importance to photonic manufacturing are several high-accuracy submicron, low-cost alignment and joining methods when using PICs that include:

1. The creation of etched v-grooves in a <100> silicon optical bench for fiber attachment and creation of fiber arrays.
2. Optical fiber splicing
3. New processes under development or to be developed include:
    a. The addition of TSVs in silicon or platforms including silicon, glass, InP, etc.
    b. Wafer fabrication processes that enable fabricating electronic and photonic devices on the same wafer.

Assembly equipment is commonly requested to be able to align parts to < 0.1 micron of accuracy. Currently readily available equipment for single mode within the price range of $100,000 to $1,000,000 only achieves 0.5 micron accuracy, hence needs improvement. Many approaches are being investigated to minimize the need for such tight tolerances but still have low optical coupling losses and avoid expensive (because it is slow and requires expensive equipment) active alignment where the optical chain is activated and used to actually ensure alignment is adequate.

To capitalize on the resulting equipment, other steps are needed; overall design, inclusion of fiducials and reference points, selection of stable joining methods and joining materials, etc. In addition improved interfaces to equipment are needed to reduce programming, set-up and change over times to minimize the cost for building high mix low volume optical products.

Figure 1. illustrates a complex optical electronic heterogeneous assembly that includes PICs and related interconnects as well as multiple conventional electronic components. This figure illustrates many of the parts and implied assembly issues that arise using PIC and combining them with complex electronics.

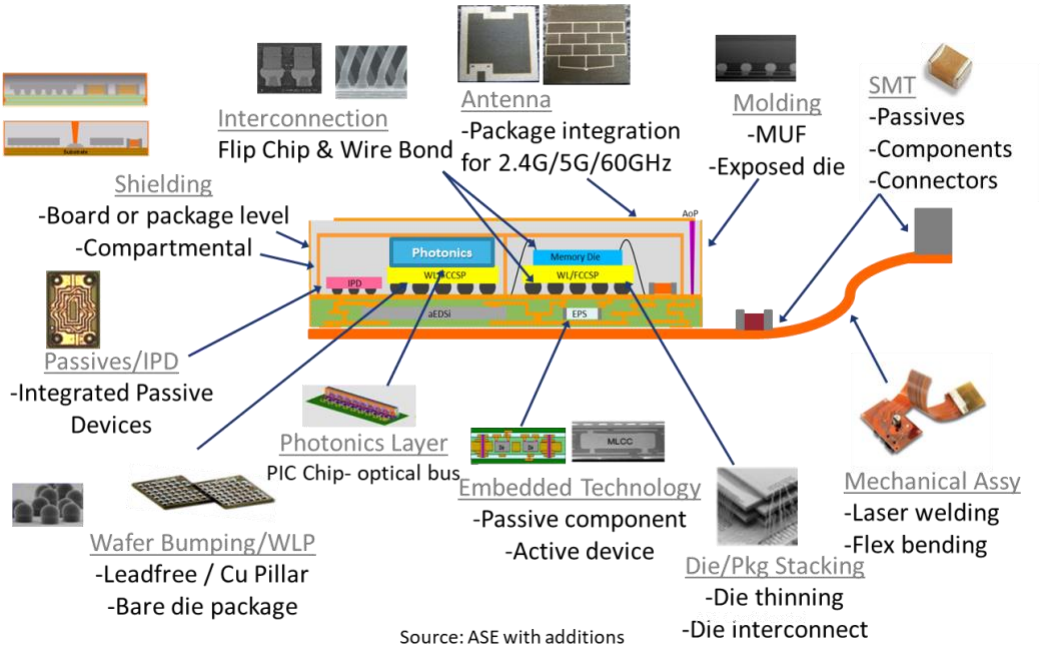


***Figure 1**. Heterogeneous integration vision to incorporate photonics functionality.*

Optical test is complicated by the need to provide not only optical sources and detectors but usually similar electronic functions as well. The testing of 10 to 100 GHz speed of many optical devices requires expensive test equipment. In addition, optical signals have many parameters that need to be both generated and measured; wavelength, power, modulation rate, modulation method, polarization, etc., often for many channels simultaneously. 12 channels are common today with roadmaps forecasting over 1024 channels in the future. Providing all those sources and detectors results in complex, expensive test sets.

SITUATION (INFRASTRUCTURE) ANALYSIS

In this section the current situation of the assembly infrastructure is analyzed. Starting with best practices for designs, followed by the manufacturing processes and available equipment. Also the quality, reliability environmental issues and test, inspection and measurement will be discussed.

Design Requirements

Low cost, high performance optical products start with good design. Good design for optical devices requires:

- Minimizing the number of parts
- Choosing parts that are adequate but not overly specified
- Minimizing the number of assembly steps
- Utilizing massively parallel fabrication and assembly methods such as wafer fabrication, die-to-wafer bonding or even wafer-to-wafer bonding rather than part-by-part placement and joining
- Understanding details of parts and working with manufacturers to ensure the parts chosen have:
    - the necessary dimensional consistency
    - suitable location reference points
    - surfaces to which suitable joints can be made
    - shipping package containers that interface with manufacturing assembly equipment (i.e. in tape and reel, waffle pack, etc.)

- Evaluating the extremes of part specifications and dimensional tolerances to ensure the design will be robust
- Maximizing the tolerances required as best as possible
- Ensuring that dimensional requirements can be achieved by ensuring that:
    - fiducials and other reference points are adequate for the tolerances desired
    - joining methods and materials are compatible with the dimensional and tolerance requirements
    - suitable manufacturing equipment is available to assemble the parts

A specific and important design parameter for optical products, especially those utilizing SM technology, is evaluation of the dimensional variations inherent in both the assembly process and the operating environment over the life of the product. Maintaining location consistency of 0.1 micron for optical chains that often have dimensions of 10 mm, or so, requires avoiding movement due to mechanical stress, temperature changes, temperature gradients, aging, cold flow and other phenomena. This implies avoiding changes in the optical chain greater than the 0.1 micron required over the 10 mm, or 1 part in 100,000 (that is equivalent to 1 mm over 100 meters, a distance a little longer than an American football field).

Achieving this degree of stability requires consideration of the properties of the materials (thermal expansion coefficient differences, the modulus of the materials, material strength, Poisson's ratio, etc.), and assembly process temperatures of 85 ℃ to as high as 250 ℃, environmental stress testing from -40 ℃ to +125 ℃, shock to 1000 G etc.

The behavior of materials under these conditions is governed by the Generalized Hooke's Law listed in Appendix B. These equations relate Young's modulus, Poisson's ratio, temperature and the thermal coefficient of expansion, to stress and strain. These equations imply several important things:

1. When temperature changes, something moves or the stress increases at a rate established by the coefficient of expansion and Young's modulus.
2. When something is stretched or bends, thus changing strain, stress increases in accordance with Young's modulus.
3. A higher Young's modulus implies less motion with strain or temperature changes.

These generalizations make the point that achieving stable, accurate known dimensions through the manufacturing process and environmental stress over the life of a product requires taking into account these detailed material properties.

One result of these issues is the need and benefit from using high modulus materials such as ceramic, glass and metal, ideally with low thermal expansion coefficients. These high modulus materials minimize relative part movement under stress and temperatures changes, are not as susceptible to property changes and corrosion from exposure to the environment and do not exhibit major phase changes in the manufacturing and use temperature ranges, all of which are minimize mechanical movement. Another benefit of these materials is that they often provide a sealed hermetic environment that minimizes

Generalized Hooke's Law
Appendix B describes the behavior of materials when they are stressed, strained, or their temperature changes. These equations and their implications drive the deformations and shape changes that occur in material and combinations of materials due to temperature and stress or strain changes. While they may look complex, they are relatively simple. For example, when the temperature of a material changes the length of that material changes due to TCE, or, if the material is constrained in one or two dimensions and cannot move freely, the stress will change with Young's modulus and the material shape will change in the unconstrained dimensions by an amount set by Poisson's ratio. In more generalized combinations of conditions, the equations describe bending, shear stresses, etc., and can be used to predict motion that exceeds the elastic limit resulting in failure or permanent deformation, for example.

environmental effects. As a result, this technology is referred to as hermetic packaging.

Unfortunately, hermetic packaging tends to be expensive. Thus engineers are moving to lower cost materials and methods that usually incorporate organic materials. The organics have lower modulus and thus move more with stress, have higher coefficients of expansion (up to 10 times) and move more with temperature changes, and lower thermal conductivity leading to temperature gradients that induce stress and hence movement. The resulting shape changes are often not simply an increase in X, Y or Z but some complex mix resulting in warping, "saucering" or "potato chipping".

One of the more demanding mechanical requirements is maintaining planarity especially due to the requirement that modern electronic products be "thin" meaning a few mm thick. Parts about a millimeter thick are not inherently stiff and easily become non-planar if larger than few centimeters. This is an important issue in reflow soldering of micro ball grid arrays for example.

Assembly processes often introduce materials to form joints between parts; epoxies, solders, adhesives, etc. The properties of these materials are as important to dimensional stability as the properties of the basic parts. This issue is addressed further in a later section and table of joining methods.

The choice of substrates and other functional materials in the assembly or package is based on their specific properties as depicted in **Figure 2.**

	Kovar	Copper-tungsten	Alumina	Aluminium nitride	Silicon	Gallium arsenide	Indium phosphide
Expansion coefficent	5.8 ✓	~7 ✓	4.9 ✓	4.5 ✓	2.6 ✓	5.8 ✓	4.5 ✓
Thermal conductivity	17 ✗	~180 ✓	32 ✗	~170 ✓	150 ✓	40 ✗	60 ✗
Mechanical stability	✓	✓	✓	✓	✓	?	?
Reliability	✓	✓	✓	✓	✓	?	?
Scales to micro-packaging	✗	✗	✗	✗	✓	✓	✓
High-speed electrical	✗	✗	✓	✓	✓	✓	✓
Bonding of chips, passives, IC's	✗	✗	✓	✓	✓	?	?
Precision location features	✗	✗	✗	✗	✓	?	?
Batch manufacture	✗	✗	✓	✓	✓	✓	✓
Batch population	✓	✓	✓	✓	✓	✓	✓
Waveguides	✗	✗	✗	✗	✓	✓	✓
Maturity	✓	✓	✓	✓	✓	✗	✗

Figure 2*. Materials properties and choice for use in a photonic package (courtesy Entropix Ltd, Bob Musk 2014)*

In summary, these phenomena make holding dimensions in products to 1 part in 100,000 challenging. The use of finite element analysis and Hooke's equations can often elucidate these changes and enable the engineer to make suitable choices.

The critical questions to ask related to assembly before the design is finalized are:

- Are the locations on parts that need to be accurately located with respect to one another well defined by features the equipment can use as a reference?
- Is the assembly equipment able to find the location of these critical points on the parts to be assembled?
- Is the equipment able to move the parts into position with respect to one another with the needed accuracy?

- If joining materials are used, will they adhere to the part surfaces?
- Are the surfaces to be joined flat and coplanar enough to be joined?
- Will the joining temperatures and thermal profile distort the joint irreparably?
- Will all of the materials survive the assembly and operational environments and retain the desired location tolerances, especially during thermal cycling?

Parts To Be Assembled

Optical devices are likely to utilize the following parts that will be assembled utilizing the joining methods and equipment noted above:

- Passive optical components
  - Lenses
  - Mirrors
  - Isolators
  - Optical connectors / interfaces
  - Fiber, both SM and MM.
    - Single fibers
    - Ribbon fiber: i.e. 4, 8, 12, 16, etc. fibers
  - Planar waveguide Structures with
    - Embedded waveguides
    - Gratings
    - Multiplexers
    - De-multiplexers
- Active Optical devices
  - Lasers
  - Photodetectors
    - PIN diodes
    - Avalanche diodes
  - Mach Zenders or other modulators
- Electronic devices
  - Electrical connections and connectors
  - Semiconductor chips
  - Passive components such as resistors, capacitors, etc.

These components are assembled on a variety of substrates or platforms including the following:

- Conventional FR-4 or FR-5 Circuit boards
- High frequency circuit boards using Rodgers 4300 dielectric, for example

- Glass substrates with waveguides, optical vias, gratings and other features
- Silicon substrate with TSVs, electrical traces, optical waveguides, optical vias, gratings, possibly some active components such as detectors, etc.

These parts are assembled using a variety of assembly and joining methods as described in the following sections.

Pre-assembly Processes

Wafer Thinning

Device wafers from the semiconductor fabs are as thick as 750 µm to provide mechanical strength during wafer fab processing and handling. These thicknesses are too high for most new applications requiring miniaturization and portability so wafer backgrind, or thinning, has become a common step to provide the thin die desired for advance packaging. Backgrinding is usually the first step in the assembly packaging process.

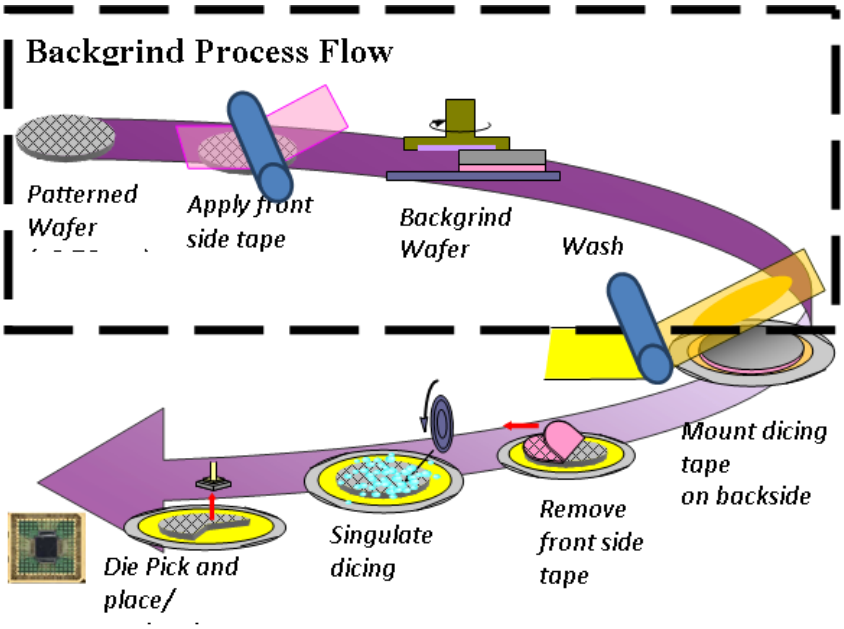


***Figure 3**. The backgrinding and dicing process flow with backgrinding highlighted in the dash box.*

The typical wafer backgrinding flow is shown in **Figure 3.** within the dashed box. Wafer backgrinding is an established industry practice that utilizes grinding wheels shown in **Figure 4.** & **Figure 7.** with teeth on highly automated machines such as the DAG 810 in **Figure 5.** using counter rotating chucks as shown in **Figure 6.** High adhesion tapes are used to temporarily hold the wafers firmly during grind to any desired thickness. Thinning by grinding is usually a two step process with a rough grind using an ~400 grit for the bulk of the removal, followed by a fine grind with an ~2000 grit to remove a final ~1 µm in thickness. An additional wafer polishing or etching step to provide a mirror finish after the fine grind may also be performed to reduce residual stress and increase strength by removing micro cracks.

With the variety of wafer materials used for photonic devices, proper grinding wheel selection is key to successful grinding III-V or II-VI materials.

The diamond embedded grinding wheels are a consumable. The binding material ranges from resin to metal to vitrified depending on the application. Each grinding wheel has a lifetime of several thousand wafers before the teeth become bare and the wheel has to be discarded. See the nearby table from Disco listing grinding wheels for different types of wafer materials.

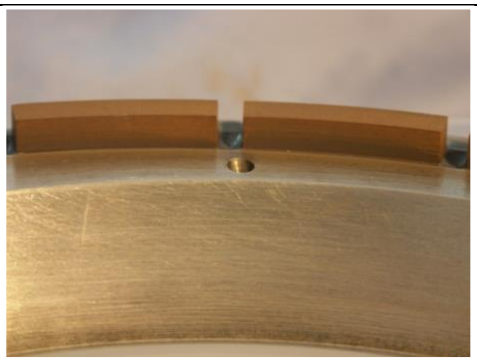


Figure 4. *Edge of typical grinding wheel.*

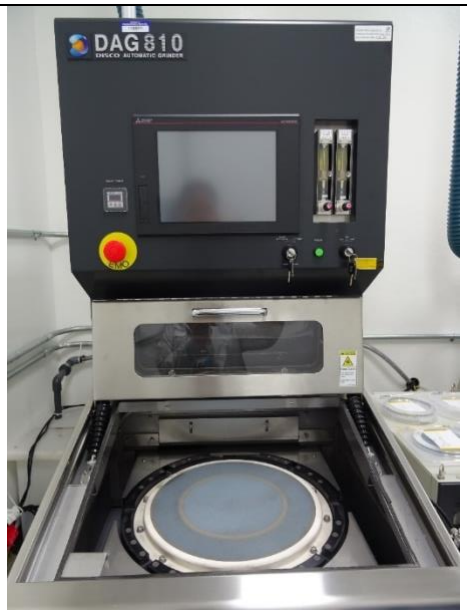


Figure 5. *Backgrinding machine.*

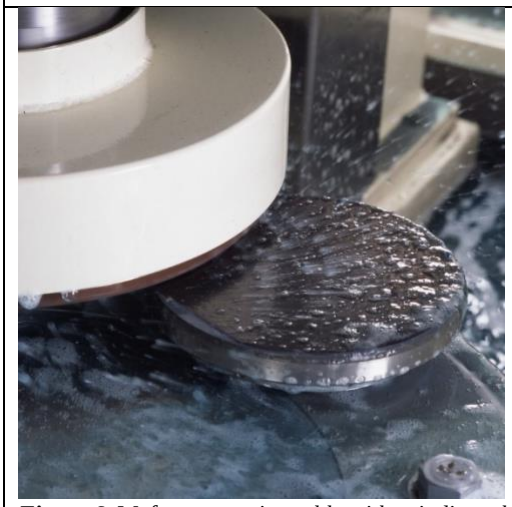


Figure 6. *Wafer on rotating table with grinding wheel to the upper left.*

Figure 7. *Typical grinding wheels.*

Material	Typical Wheel Type to Use		Bond Type		
	Z1	Z2	Resin	Vitrified	Metal
Si	#320-BT300	#2000-BK09, #2000-BR361 #4800-VV4B, Poligrind	YES	YES	NO
GaAs InP	#600-BK01	#2000/#4000-BR199 #2000/#4000-BR440 #2000/#4000-BR328	YES (Soft Resin)	No	NO
Borosilicate Glass	#240-BR385	#1000/#1500-BR385 #2000-V631	YES	YES	NO
Sapphire	#280-M132	#1400-Metal #1400-V667	NO	YES	YES
GaN	#600-M236 #600-V469 #600-V495	#2000-V643 #2000-V631 #2000-V667	NO	YES	YES
SiC	GS08-S10111	GS08-SI0124 #2000-V631	NO	YES	YES
LT/LN	#1000-V401	#3000-V643 #6000-V643	NO	YES	NO
PZT	#600-BR111 BR448 or BT300, etc. (Depends on incoming condition)	#1000-BR111 #2000-BR440 Poligrind	YES	YES	NO

Figure 8. *Overview of typical wheel and bond types per substrate material*

High precision machines have the capability to thin wafers to < 25 µm in thickness. The total thickness variation across the finished wafer can be as low as ± 2 µm. Ultrathin silicon wafers, as thin as 25 µm in thickness, are widely used commercially for devices such as memory chips. These thin chips are fragile, but innovative processes are now available to strengthen the chips by smoothing the surface and adding temporary support wafers for handling during assembly and other processing. For die thickness greater than 100 µm, conventional pick and place methods are still useable. Specialized release processes are required to pick up the thinned die.

Some of the possibilities for stress relieving wafers after grinding are shown in **Figure 9.** below.

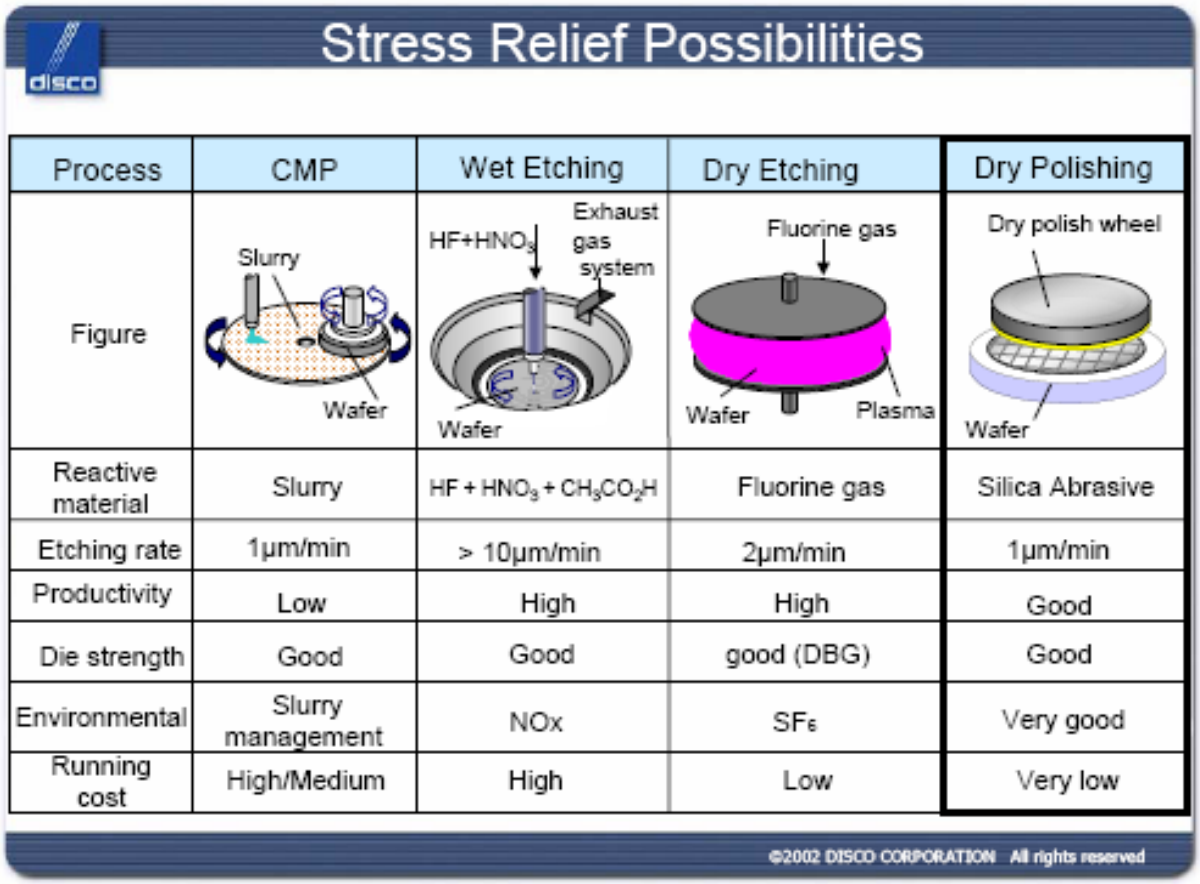


Figure 9. *Post grinding wafer stress relief options*

Fortunately, machines have been designed with a universal vacuum chuck that can hold 6" or 8" or 12" wafers without change overs.

Wafer singulation of individual die

Multiple techniques to singulate wafers have been developed over the years and continue to evolve. Scribe and break was the original method used with small 2" wafers and it is still used today for those wafers as well as expensive materials where elimination of the kerf increases die count.

Sawing is most commonly used today and has evolved into a series of highly sophisticated methods, some of which are described in Appendix D. Laser dicing and plasma dicing have evolved and are growing in use. **Table 7.** describes these singulation methods.

Table 7. Wafer Singulation Methods		
Process	**Material**	**Comments**
Scribe and Break	InP, glass, SiGe other expensive material	Raises die count by eliminating kerf area. Multiple microns of inaccuracy in break location with respect to die features
Sawing	Diamond impregnated resin blades turning at 30,000 ± rpm with cooling water is the dominant method for most materials.	Limited to straight cuts, generally implying rectangular shapes. Generates much debris that can contaminate optical components. Often used with die attach film on wafer.
Thermal Laser Ablation	High energy photons cause material to sublimate.	Ablated material can contaminate die.
Stealth Laser Dicing	A process that thermally generate a fracture in the middle of the substrate by focusing energy there.	Expensive equipment required
Plasma Dicing	Material is removed by reactive ion etching.	Wafer must be designed for the process; no metal in dicing street and the etching sites must be defined lithographically. An emerging process that allows any shape of die with minimal debris.

Figure 10. below shows the popularity of these singulation methods over time.

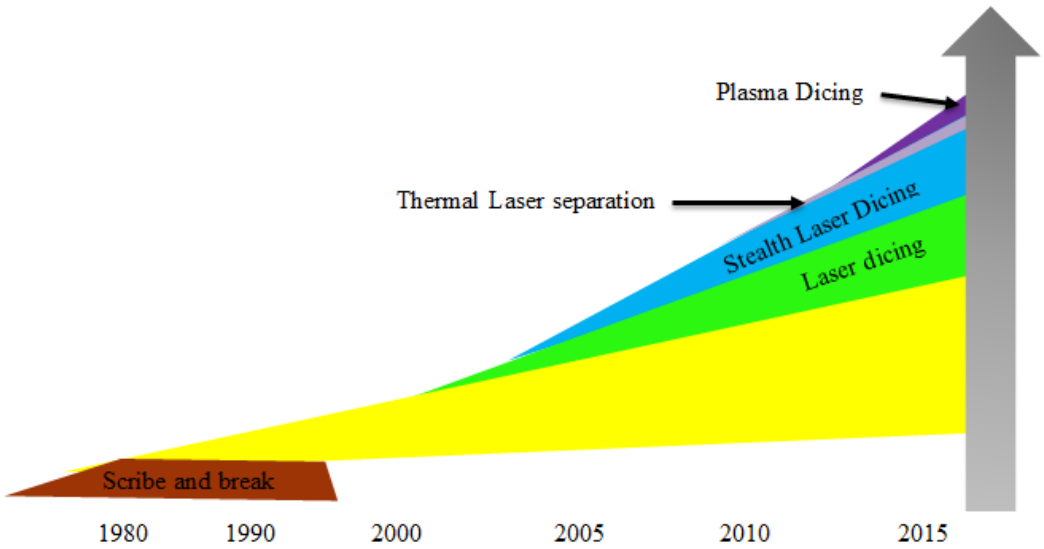


Figure 10. *Singulation methods over time*

Appendix D describes these singulation methods and their use with backgrinding/thinning, in more detail.

Die attach films

Figure 11. *DAF in rolls and with handling frames*

Die attach film is commonly utilized in conjunction with singulation where it provides a variety of functions, but most important, eliminates dispensing die attach epoxy. DAF is provided in roll or sheet form as shown in **Figure 11.** along with a wafer handling frame with which it is utilized like conventional dicing tape. DAF is supplied as a multi-layer tape that is integrated into saw singulation where it replaces the conventional dicing tape. DAF is put on the back of wafers before singulation with a layer of what will become the die attach adhesive in contact with the backside of the wafer. During singulation, the saw (or laser) cuts through this adhesive layer, but does not cut a second, lower layer that continues to hold the die in place after singulation on the dicing frame. When dies are subsequently picked for placement, this adhesive layer sticks to the back of the die but comes off of the lower layer so the die with adhesive can be placed on the surface (which is often heated to immediately B stage the epoxy) where it provides the adhesive function replacing conventional, dispensed epoxy.

DAF not only eliminates the dispense step but holds the die in place, minimizes voiding and provides uniform bond lines and good fillets with minimal "creep" up die sidewalls. Non-conductive, electrically conductive, and thermally conductive DAF materials are available in a variety of thicknesses from roughly 10 microns to 75 microns. For stacked die 3D architecture, DAF is crucial and is fully integrated into current electronic products.

Alignment and Joining Methods

Table 8. Primary Methods Used to Join Optical and Electronic Parts				
Color code Meaning	Suitable for submicron stable joints	Suitable for submicron joints if the stress is low and the joining material, if any, is thin, meaning less than a few microns.		Not suitable for submicron joints
Attach Material	**Application Methods**	**Thickness**	**Maximum Temperature**	**Comments**
Die-to-Wafer and Wafer-to-Wafer Bonding Materials/Methods				
Oxide to Oxide Bonding	No Application; careful surface preparation	Angstroms	≥ 20°C	Requires very flat surfaces
BCB Bonding	Coating with polymer			Used for wafer-to-wafer bonding
Low Modulus Organic Joining Materials				
Epoxies, non-conductive electrically, low thermal conductivity	Needle dispense, stamp, dip part, Die attach Film (DAF)	≥ 5 microns	80 °C - 200 °C	Epoxies are the most common attach material used. DAF is applied to wafers before sawing.
Epoxy, thermally conductive	Dispense, stamp, dip, DAF	≥5 microns	80 °C - 200 °C	Conductivity <40W/m- °C
Epoxy, electrically conductive	Dispense, stamp, dip, DAF	≥ 5 microns	80 °C - 200 °C	
Acrylate Polymer	Dispense, stamp	>25 microns	80 °C – 200 °C 20 °C – 80 °C	UV cured, non-conductive, good optical properties
Metallic Joining Materials				
Sn63 Solder	Paste, preform, spheres, electroplate	5 - 75 microns	195°C – 210 °C	Cold flows at 20 °C.
SAC alloys	Paste, preform, spheres	5 - 75 microns	240 °C	Alloys of SnAgCu. SAC305 is 3% Ag, 0.5% Cu, balance Sn. Many alloys used. Generally high modulus. No cold flow.
$Au_{80}Sn_{20}$	AuSn preform, clamp & heat	~75 microns	280 °C	Typically utilizes a preform. Once alloyed with a little extra gold, the melting point is higher.
$Au_{98}Si_2$	Scrub silicon die, press and heat	<25 microns	363 °C	Requires scrubbing and pressure at temperature. Hard to achieve accurate location without complex automatic equipment.
Au thermo-compression	Gold to gold with pressure at temperature	<100 microns	>150 °C	Requires > 20 grams of force per 2,000 sq. microns of area on EVERY joint. Not a strong joint.
Au thermo-sonic	Pressure with 120KHz ultrasonic	NA	>120 °C	Used for ball and wedge wirebonding.
Al ultrasonic		NA	20 °C	Used for wedge wirebonding
Braze	Reflow, controlled atmosphere	varies	650 °C	Typically done in a belt oven to join metalized ceramic and metal. Very stable joints.
Weld, laser	Spot or scanned beam	none	1000+ °C	Brief temperature excursion in a limited area

Weld, electrical	Spot or dual pinching electrodes	none	1000+ °C	Metal-to-metal in an engineered process to control part temperatures. Warpage possible.

While optical devices utilize many conventional materials, they also utilize specialized materials for specific applications. The most important differences relate to dimensional stability and maintenance of optical properties, particularly clarity, over the life of the product.

Materials with low modulus are inherently "unstable" dimensionally as stress from either temperature changes or external forces results in movement. Thus optical joining materials intended to hold parts in place tend to have high modulus.

Materials that yellow with age need to be excluded. Classic Sn63 solder cold flows under stress, moving to relieve the stress. That highly desirable property in electronic assembly is detrimental in high tolerance optical assemblies. The SAC alloys, for example, that do not cold flow, are a better choice for joints that must be stable.

Joining utilizing AuSn and CuSn is suitable for optical devices as these two systems form an alloy upon heating that is a solid above the temperature required to form the alloy. Thus, over these temperatures, the material is a solid and able to hold parts in position. The important point with these alloys is to ensure that when they reach the "activation" temperature, that the parts are located in the desired position and that the formation of the solid rigid alloy does not cause movement.

Material Properties Needed

An issue with some materials, especially organics, is finding their properties. Manufactures of materials often provide data sheets and by law must provide Material Safety Data Sheets (MSDS) that address hazardous properties. Unfortunately, the data sheets often exclude many of the properties that are important in optical design. Organics and silicones are often compounded utilizing a mixture of constituents to achieve a desired set of properties. Data on the properties of many materials is inadequate for detailed optomechanical design. Properties that are often needed include Young's modulus vs temperature, both before and after curing, CTE vs temperature, Poisson's ratio, dimensional change from water absorption and related percentage weight gain, dielectric constant and loss tangent vs temperature and frequency up to 100 GHz, etc. The Industry needs standard sets of desired material properties developed and manufacturers to then routinely provide that data.

Materials Used in Joining Processes

Most of the standard joining materials and methods used in optical products are widely known and commonly used in electronic assembly including the electronics associated with photonic products. For electronic joining applications, the long-term performance of these methods is generally adequate.

However, when the joined parts or elements must remain in place to submicron dimensions over the life of the product, only a subset of these materials and methods will suffice. In addition, some of the material and methods will provide the stability needed only if the joining material, such as an epoxy, is thin and has a high modulus. In other cases, the material and method is simply not suitable for a joint that must be highly stable.

Wafer-to-wafer and Die-to-Wafer Specialized Bonding

A relatively new bonding method used for wafer-to-wafer and die-to-wafer bonding utilizes silicon and other oxides. If surfaces are very flat, the surface of an oxide is activated, possibly with please "cleaning" a joint between two surfaces will form when the surfaces are brought into contact.

The resulting bond is quite strong. Some considerations to utilize this method include:

- Minimize waviness, bow and warp
- Utilize Inert RIE to clean surfaces and enhance surface porosity
- NH_4OH exposure terminates surface with amine groups that form bonds

- Bond energies greater than 1 J/m2 obtainable at room temperature
- Oxide deposition + Chemical Mechanical Polishing (CMP) to 0.5 nm RMS spec

The spectrum of materials that can be joined this way includes silicon-to-silicon, germanium, indium phosphide, gallium arsenide, gallium nitride, quartz, and others. The resulting bond strength typically exceeds the fracture strength of the bonded bulk materials. These methods are widely used to affix InP material to silicon to provide a direct bandgap material coupled to a waveguide in silicon to provide lasing and optical gain.

Epoxy Joint Considerations

The designer and process engineer should consider the following points when choosing an epoxy for a specific joint:

- Can the joint design meet the performance requirements when using an epoxy as the joining material?
- Does the epoxy need to be electrically, thermally conductive or non-conductive?
- What modulus must the cured epoxy exhibit?
- Will the epoxy perform as needed in the post deposition manufacturing and operating temperature environment and will the epoxy negatively impact overall product reliability?
- What is the desired epoxy bond-line thickness?
- How to prepare the joining surfaces?
- How to apply epoxy on the surfaces?
    - Manual needle dispensed in a pattern?
    - Machine dispensed by needle (time pressure, shot-piston or auger), jetting, or other?
    - Deposit on one surface by stamping?
    - Film preapplied on the part?
    - Preform?
- What percent (%) of voids is allowable in the finished joint?
- What is the required viscosity during deposition or during curing?
- What is the required time-temperature profile to cure the epoxy?

Location Accuracy with Epoxies

Epoxies shrink during curing by varied amounts, which can create accuracy issues in all six degrees of freedom.

One motion happens when shrinking of a thin layer of epoxy used to hold two parts together. The shrinking amount and uniformity can cause variations in bond-line thickness and bond-plane tilting. Epoxy application uniformity and material properties can affect the accuracy. Some designs use benching surfaces to hold the two parts at the proper bond-line and bond-plane.

Another motion happens when shrinking of epoxy fillets causes in imbalance of forces. When a fillet around a part shrinks, the shrinkage tends to pull the parts toward the shrinking material. For example, unsymmetrical fillets around four sides of a die will shift the die in the direction of most pull during curing.

Epoxies also have a relatively high TCE; from 10 to 120 often 30 to 50 ppm/^{o}C. Above the glass transition temperature, which varies from -10 ^{o}C to +240 ^{o}C but is typically 85 ^{o}C, the TCE increase dramatically, often by a factor of 4 or more to ~150 ppm/^{o}C. Designing optical devices, especially single mode devices, to function with

this amount of motion is very challenging. Hence, critical joints, meaning those that must not allow significant motion during the manufacturing and use cycle, usually exclude epoxies.

Uses of epoxy:
Some common uses of epoxies are in die attachment to hold die in place, wire bond encapsulation to provide protection, underfill to strengthen flip-chip and BGA joints, overmolding to provide environmental protection, other, specialized uses.

Modulus of Elasticity:
Epoxies with a wide range of room temperature modulus are available; from less than 2 GPa (~ 300 Kpsi) to greater than 20 GPa (3,000 Kpsi). Above the glass transition temperature (T_g), the modulus can drop by a factor of 10.

Epoxy Material Packaging:
Epoxies are inherently two-part systems, traditionally a catalyst and resin. Electronic epoxies come in two forms:

- two-part system. These are available and used but require mixing just before use and potentially de-gassing.
- pre-mixed materials that are shipped and stored cold (typically < -40 ^{o}C). They are thawed, and at least kept dry if not actually dried, just before use. Drying is needed due to the potential for water condensation if the material is not stored in a dry environment or sealed contained.

Epoxy Forms:
In addition to the two-part systems and the premixed materials shipped and stored cold at -40 ^{o}C, epoxies are sometimes available as films. These films are very attractive in electronics for reasons explained below and of value in optical products.

Epoxy pastes and liquids:
After the epoxies are mixed or thawed, they are deposited on substrates using needle dispensing (time-pressure, auger), jetting, or stamping (like a classic hand stamp that might say "sold") to give specific shapes and a controlled quantity. The viscosity is important to controlling flow. Some epoxies have a high viscosity and stay exactly where they are placed, others, used for underfill or encapsulation have low viscosity and whose flow is thus influenced by capillary action or gravity.

Epoxy films:
The epoxy films are typically applied on the back of wafers before dicing as a B-staged. After dicing the part, typically die, are aligned and placed on a heated substrate where the epoxy undergoes further curing holding the parts in place. The uniformity of the thickness, distribution and shape control result in highly predictable final part location.

Epoxy Pot Life:
Epoxies have varied pot life. Long pot life is good for manufacturing environments where material can be used over an extended period without the properties, especially viscosity, changing significantly and effecting the dispense pattern and subsequent flow. Some heavily loaded epoxies, such as those that have high thermal or electrical conductivity, contain a high percentage of volatiles that evaporate resulting in a short pot life.

Epoxy conductivity:
The three basic types are:

- Electricaly conductive
- Thermally conductive (< 40 W/m ^{o}C)
- Non-conductive

Solder joints
Solder is used primarily to make electrical joints and is not very suitable for mechanical joints. Nonetheless, solder is sometimes used for that purpose, especially in conventional surface mount assembly technology where the mechanical stresses are minimal.

Solder alloys and their properties:
Many solder alloys with varied properties are in use. The classic solder is Sn63, meaning 63% tin and 37% lead by weight. It has excellent properties for electrical joints but has fallen out of favor in recent years because of its lead content (lead can cause problems in biologic systems and is being eliminated from use in a variety of applications including electronic soldering under the RoHS regulations passed in many countries). A common Sn63 replacement is the SAC alloys, alloys of tin (Sn), silver (Ag) and Copper (Cu). The designation SAC 305, for example, means an alloy of 3% silver, 0.5% copper and the balance tin. Variations on this combination are common as is the use of other alloys containing Bismuth, Indium, etc.

In addition to eliminating lead, alloys are chosen for their cost, melting point, wetting characteristics, mechanical and electrical properties, sensitivity to tin whisker growth and other properties.

Classic Sn63 solder has the interesting property that it cold flows. If Sn63 is under mechanical stress, it will slowly flow to relax the stress (a piece of solder wire with a weight hung from it will slowly stretch). This property is good in electrical joints because the joints self-relax rather than break under stress. The latter is bad, of course, because breaking implies a complete separation of two parts that were joined resulting in an electrical open circuit. This cold flow property means that Sn63 is not good for mechanical joints that bear stress. Thus, classic electrical joints always had a mechanical connections that was supplemented by solder to form a metal-to-metal continuously conducive electrical joint.

The cold flow property of Sn63 implies that that alloy is not particularly good for optical devices when mechanical stability is important. If any stress is placed on the joint, parts will move to relieve the stress potentially interfering with the optical functions.

The SAC alloys, however, do not cold flow and tend to be more brittle.

Solder Fluxes:
Solders must “wet” the surface of conductors to make a good intermetallic joint. Wetting is enhanced by cleaning conductive surfaces and removing oxides. The most common method of doing so is by using a “flux”. Flux removes oxides and other surface contaminants so the liquid solder can come in direct contact and thus wet metal surfaces. In addition to being clean, the metal surface temperature must be above the melting point of the solder so the solder will stay in the liquid state.

Flux can be applied to the interfaces to be soldered in multiple ways. The most common is to mix a mild acid with an organic carrier and solder in the form of small balls to form what is called “solder paste”. This material can be deposited with stencil printing, screen printing, needle dispensing, etc.; basically, any method that puts the material where it is needed to form a joint. The most common method in electronic assembly is stencil printing; typically using automatic machinery.

In addition to applying flux in a paste, flux can be applied as a separate liquid, which is sometimes done by putting the flux in the center of a wire made of solder. Hand soldering often utilizes that method of a flux applications. Wave soldering, and fountain soldering are processes that make a “hump” or “high spot” of melted hot liquid solder

by pumping the solder. Flux is often applied as a foam or liquid. The advantage of the "solder hump" is a board, for example, can be moved over the "hump" without touching anything but the liquid solder.

A final method of applying "flux" is with a gas such as forming gas, 4% hydrogen, 96% nitrogen, with formic acid. These agents are strongly reducing and convert metal oxides back to base metal to enhance their wettability.

In the case of the liquid or paste fluxes, they tend to leave a residue that can be detrimental both cosmetically and functionally. Thus, methods of removing this residue are inherent in soldering processes. The most common flux removal process is washing with de-ionized water. The flux system, of course, must be compatible with that process. Sometimes, saponifiers (soap) is often mixed into water to enhance the cleaning power of the water.

In electronic assembly, solder pastes referred to as "no-clean" are often used to eliminate the final washing step and issues associated with it. These solders leave behind a residue that is cosmetically detrimental, can affect high frequency dissipation factor and potentially contaminate optical surfaces. Thus, the no-cleans are not recommended for optical products unless they are cleaned, an increasingly common practice!

Solder Joint Location Accuracy

The following issues must be addressed to maintain accurate part location in soldered joints. When solder melts and reflows, parts can "float" and thus move, under capillary action to an equilibrium location established by the solder thickness and the extent and degree of wetting of both the substrate and the part (also, without some sort of solder stop, such as solder mask, solder can "wick" along a metal trace causing a part to move with it).

When parts go through a reflow oven as they do in the standard surface mount process, the paste decomposes cleaning the surfaces, the solder melts so the parts being soldered are no longer held in place by the sticky solder paste. Thus, not only capillary action and "floating" can move parts but so can air flow or the mechanical motion of a moving belt that "jiggles" parts while the solder is wet causing them to move. Thus, accurately placing parts during the conventional surface mount process is only part of the process of fixing parts with high accuracy in desired locations. The steps, after placement of transporting and reflowing the solder, need to be carefully considered to give high accuracy, repeatable results.

Finally, as solder solidifies, it shrinks a small amount thus causing further movement that may need to be considered for high accuracy optical devices.

High Accuracy Submicron, Low Cost Joining Methods

Processes to achieve less than 0.1 micron alignment are not generally available. Processes, including the geometries, materials, joining methods and equipment to implement higher accuracy assembly are needed and under development. Methods being explored include the use of capillary action to move small parts into position, the use of silicon optical benches, i.e. silicon substrates with features such as "stops" and barrier fabricated as required to submicron location tolerances that serve as physical stops and thus act as locators.

As noted above, a very important need to reduce cost of optical devices, especially single mode devices, is to eliminate active optical alignment. Thus, an emphasis on that need is inherent in much that follows. Specifically, emerging optical devices that utilize SM technology require high accuracy (<0.1 microns) and low cost (implying a few seconds of time on equipment) joining methods.

Standard joining methods capable of fulfilling this high accuracy need are:

1. Metal deformation bonding
2. Eutectic bonding with AuSi, AuSn, Cu Sn or other similar metallurgies.
3. UV cured polymers such as acrylates
4. Spot or laser welding

5. Si to Si bonding
6. New processes under development or to be developed

The following sections expand on these methods.

Metal Deformation Bonding

If two clean metal surfaces are put in contact with one another and then deformed so as to at least double the area of the surfaces that touch, many metal combinations will bond and form a strong intermetallic joint. Some combinations of metals require higher temperatures, scrubbing of the surfaces mechanically or ultrasonically, or a controlled environment, usually meaning excluding oxygen. While the most common use of this technology in electronics is wire bonding [1], the processes can be used for other types of joints. This basic technology has the important advantage that it is fast; wire bond joints can be made at rates greater than 10 per second.

The following **Table 9.** provides details of some of these common processes that are used for wire bonding. While the table is specific to wire bonding, these same physical processes will work with other types of parts and provide the strength and speed needed for optical devices. Unfortunately, equipment to implement that type of bonding in optical devices is not readily available but could be developed.

Table 9. Metal-to-Metal Joining Methods

Process	Temperature	Pressure	Common metal combinations	Other Comments	Environment
Ultrasonic wire bonding	20 °C	yes	Al to Ag, Al to Au		air
Thermosonic wire bonding	150 °C	yes	Au to Al, Au to Au, Cu to Cu	120 KHz ultrasonic scrubbing	Air. At least N2 for Cu to Cu, forming gas preferred
Thermo-compression bonding	150 °C	~ 20 gms per 500 sq. microns	Au to Au		Air but often aided by N2 or forming gas

Eutectic Bonding

Some alloy systems have the interesting characteristic that when the two metals are heated in contact with one another to temperatures well below their individual melting points, they will diffuse into one another and form an alloy. The Au + Sn, Au + Si and Cu + Sn systems all have this property. These metallurgies can be implemented for use as a joining method by a., making parts out of the two materials, b., depositing these metals on the surface of parts to be joined using electroplating, sputtering or alternate deposition means c., utilizing a preform of one of the metals and then bringing them together and joining the parts with suitable pressure, temperature and gaseous environment if needed. After the joining process is completed, the remelt temperature of the new alloy is greater than the joining temperature resulting in a rigid joint that is formed quickly. This process stabilizes the joint.

UV cured Polymers such as Acrylates

These materials are widely used in optical devices because the process is fast, the materials are transparent to a broad range of wavelengths, and are relatively easy to use. Further curing with heat is also possible for these materials. Thus, a common practice is to “tack” parts in place with a “dab” of acrylate, expose it to enough UV to make a temporary joint, then remove this sub assembly from the primary joining equipment and complete curing the acrylate with more UV or heat.

One consideration and potential limitation is that common to many polymers. Young’s modulus is relatively low and the TCE of the cured materials is relatively high implying that the material will move a relatively large amount

with temperature changes or stress compared to metals and ceramics. These phenomena must be taken into account during the design stage.

Spot or Laser Welding

Welded joints are formed by bring two pieces of metal into contact and heating them hot enough so that at least one, and preferably both, pieces of metal melt, flow together, and then cool to form an intermetallic joint. Welding usually provides highly accurate positioning because the parts can usually be held in the desired location with respect to one another during the entire heat, melt, cool, solidify process. Welding methods include spot welding, seam welding and butt welding, all of which use high current introduced to the parts to be welded using heavy electrodes.

Another method of introducing heat is with a laser beam. This can be a highly controlled highly accurate process but requires more expensive equipment than high current resistance welding methods.

An issue for high accuracy welded joints is motion during cooling. Welding requires exceeding the melting point of the metal which varies, of course, but often ~1000 ^{o}C. Motion can take place before the liquid metals solidify and then during cooling from the melting point to room temperature. Avoiding these motions requires good joint design and fixtures.

Wafer-to-Wafer and Die-to-Wafer Bonding

Another assembly process of growing interest to industry, including the optical community, is wafer-to-wafer bonding. These processes are used to:

1. Fabricate a stack of wafers that have different functionality or even different materials. The stack enables processing large number of devices on a wafer in parallel to reduce cost. After the stack is built the stack is often processed further to ad other parts or features and then singulated.
2. Provide a carrier wafer to enable processing of a second wafer that might be fragile or hard to handle by itself. After processing the carrier is removed utilizing either heat, light or force.

The basic bonding technologies used for wafer-to-wafer bonding generally work with die on wafer bonding. Thus conventional die placement tools can be used with the below bonding processes to attach die to wafers.

The basic bonding technologies are listed in the table below [2], **Table 10.**

Table 10. Some Processes used for Wafer-to-Wafer or Die-to-Wafer Bonding

Process Name	Description of Process
Oxide-to-Oxide Bonding	Very flat surfaces of materials such as semiconductors or metals each have thin oxide layers that will bond when they are brought into contact, often with some heat and pressure so that they bond. (See the more detailed description of this important process below this table.)
Adhesive Bonding	A variety of organic adhesives and polymers including epoxies, dry films, BCB, polyimides and UV cured compounds are available and in use.
Anodic Bonding	Involves encapsulating components on a wafer by means of ionic glass. In triple-stack bonding, three layers (i.e. glass-silicon-glass) are simultaneously bonded.
Eutectic Bonding	Utilizes the special properties of eutectic metals that are similar to soldering alloys. These metals melt at low temperatures and allow planar surfaces to be achieved.

Fusion Bonding	The surfaces to be joined are polished to make them hydrophilic. Then they are placed in contact and heated to high temperature. Plasma pretreatment allows substrates to be bonded at room temperature.
Glass Frit Bonding	Glass frit is screen printed onto the bonding surfaces, then heated with the surfaces in contact so they are mechanically joined upon cooling
Hybrid Bonding	Thermocompression bonding of two metallic layers with an integrated fusion bond to form both an electrical and mechanical joint at the same time.
Metal Diffusion Bonding	Cu-Cu, Al-Al, Au-Au and other metallic combinations are cleaned, placed in contact and heated to form both an electrically conductive and mechanical joint.
SLID Bonding	Solid-liquid inter-diffusion utilizes diffusion and mixing of different metals to form an alloy whose melting temperature is higher that the bonding temperature.

The following *in italics* is from the Ziptronix web site. It is reproduced here as it provides a good overview of this unique technology. While Ziptronix presents the technology for wafer-to-wafer and die-to-wafer bonding, the technology may be useful more broadly.

Direct Bond Interconnect (DBI) combines a room or low temperature, non-adhesive covalent bonding technique with integrated high-density interconnect formation. DBI makes possible 3D circuits and tiled wafers with the highest performance and lowest cost available, for silicon, III-V or other materials. Unlike other 3D fabrication methods, no wire bonding, solder bumping or pressure are required, and through-silicon vias eliminate large-area design exclusions.

DBI begins with CMP to planarize the surfaces of the materials to be bonded. The CMP also exposes the respective buried interconnect connection points, or TSV. Following CMP, a thin layer of silicon oxide (SiO_2) is applied to both surfaces, which are aligned so the Supercontact points will meet. The oxide is activated to create a direct spontaneous covalent bond formation. It exceeds the fracture strength of the bonded materials.

The bond energy between the surfaces is very high and brings the TSV into contact close to each other to form effective electrical connections.

Their low resistance enables better power efficiency and reduces the overall power consumption of the 3D system. Because the process is completed at room or low temperature, there are no residual stresses, such as can occur with thermal or anodic bonding methods, nor are there epoxies or other materials that require curing. The bond also is hermetic.

Assembly Strategies

This section covers assembly strategies for several sub-assemblies. There are several considerations taken into account relating to cost of manufacturing, cost of assembly, size, weight and power consumption of the assembly, (guaranteed) performance and expected volume to be produced. These considerations will eventually determine the design and assembly strategy of the photonic modules and the system architecture. An important choice is the choice for (as much as possible) integrated functions on a single chip, the **monolithic approach**. On top of that, existing (micro-electronics) silicon foundries, like Global Foundries, TSMC, and IBM, prefer a *zero-change* approach, which means manufacturing of integrated photonics components without making any changes to the CMOS process, hereby leveraging the access to the high-volume manufacturing, test and assembly equipment which has reputable capability to produce low-cost integrated circuits.

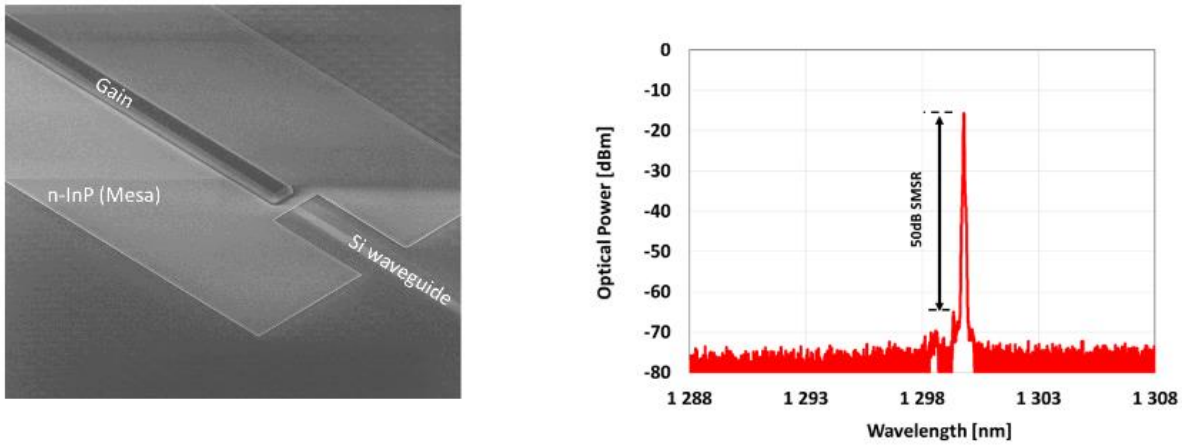
A second strategy is to produce a **heterogeneously manufactured chip**, where different materials (wafers or partial wafers) are bonded and several (high volume) front-end process steps are completed on the *sandwich*. The wafer,

3D-waferstack, is diced after processing and singulated 3D-chipstacks are obtained. Recently LETI and EV Group achieved a bonding accuracy of electrical copper contacts, sub-1.5-micrometer-pitch, over the full 300 mm wafer. In fact, this strategy is already a hybrid strategy since it bonds copper contacts *and* the in-between oxide areas from the bottom wafer to the copper contacts *and* the in-between oxide areas from the top wafer.

A photonics example of heterogeneous integration was reported by LETI (7 December 2017), who has integrated hybrid III-V silicon lasers on **200 mm wafers** using standard CMOS process flow. This shows the way to transitioning away from 100 mm wafers and a process based on bulk III-V technology that requires contacts with noble metals and lift-off based patterning. The project, carried out in the framework of the IRT Nanoelec program, which is headed by Leti, demonstrated that the hybrid device's performance is comparable to the reference device fabricated with the current process on 100mm wafers. The fabrication flow is fully planar and compatible with large-scale integration on silicon-photonic circuits. The integration required managing a thick silicon film, typically 500 nm thick, for the hybrid laser, and a thinner one, typically 300 nm, for the baseline silicon-photonic platform. This required locally thickening the silicon by adding 200 nm of amorphous silicon via a damascene process, which presents the advantage of leaving a flat surface favorable for bonding III-V on silicon. The laser can be integrated on a mature silicon photonic platform with a modular approach that does not compromise the baseline process performance.

The novelty of the approach also included using innovative laser electrical contacts that do not contain any noble metals, such as gold. The contacts also prohibit integration lift-off-based processes. Nickel-based metallization was used with an integration technique similar to a CMOS transistor technique, in which tungsten plugs connect the device to the routing metal lines.

Next steps include integrating the laser with active silicon-photonic devices, e.g. a modulator and photodiode with several interconnect metal levels in a planarized backend. Finally, III-V die bonding will replace III-V wafer bonding in order to process lasers on the entire silicon wafer.



Tilted scanning electron microscopy view of the III-V/Si DFB laser after the IIIV patterning steps.

Laser spectrum at 160 mA injection currents

***Figure 12**. Reported breakthrough by LETI, December 7, 2017, on their 3 mW optical power heterogeneously integrated laser on 200 mm silicon wafer*

Recently, at ECOC 2016, NTT Docomo presented their fabrication of heterogeneously integrated array of direct modulated InP lasers for telecom applications, including a tapered InP waveguide section and a SiON on-chip spot size converter to achieve low-loss fiber-to-chip coupling and 0.7 mW fiber-coupled output power.

The third strategy is the **hybrid strategy**, where different components and materials are, or inevitably need to be, connected/assembled. In the following sections, several assembly interfaces and assembly steps are considered:

1. Hybrid chip-chip assembly

2. Fiber splicing
3. Optical bench
4. Creation of fiber arrays
5. Fiber assembly, chip-fiber (array) assembly, die-to-die attachment
6. Planar free space coupling of waveguides to photonic circuits.
7. Non-planar free space couplers, gratings, and mirrors

Hybrid Planar Coupling of InP Chips to Silicon Nitride Waveguide (LioniX International)
An example of a hybrid architecture is depicted in **Figure 13.** This design envisions a full monolithic integration of modulators, detectors and laser on a single InP chip, the tunable laser and a low-loss beamforming network monolithically manufactured on a silicon nitride (TriPleX) chip. This assembly acts as a black box, a full RF-to-RF, one (1) signal on the modulator to sixteen (16) signals on the detectors.

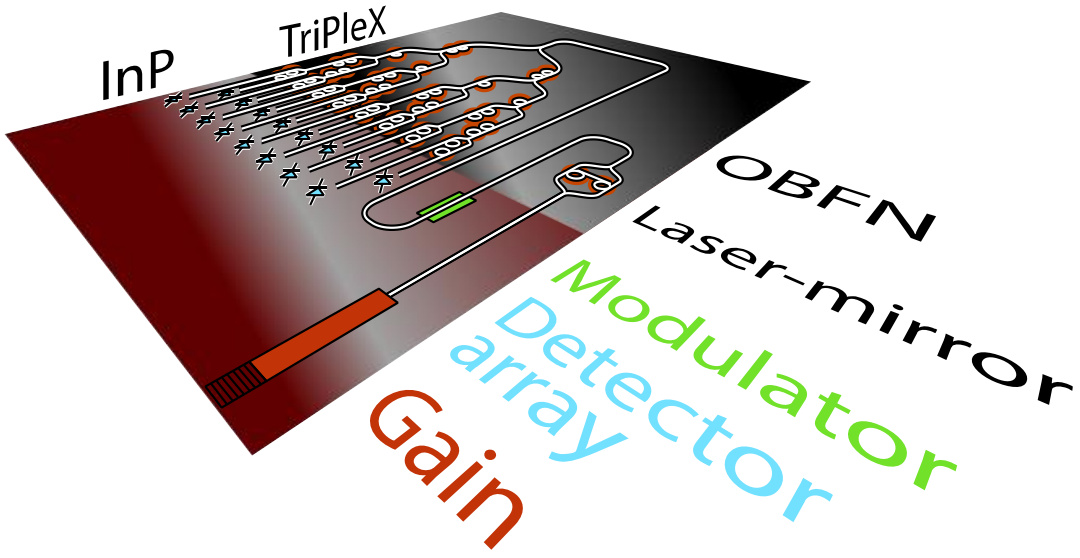


Figure 13. *Example of an architecture of an optical beamforming network with InP-TriPleX chips, after Roeloffzen et al. [3]*

In a real life demonstrator we considered several issues, to mention:

1. Cross talk on the InP chip between laser and detectors
2. Challenge to manufacture lasers, modulators and detectors in a monolithic process
3. The need for optical test ports requires interfacing with fibers or fiber arrays
4. The high frequency interconnects (10 or 15 GHz) need careful design and assembly to avoid parasitic effects that hamper proper signal detection.

An example of an optical beamforming network is depicted in **Figure 14.** The propagation losses in InP (expected 5 dB/cm) and parasitic losses of modulators, are neglected in the evaluation of the link budget.

We use an external laser with 80 mW (+19 dBm) which enters the assembly through a fiber-chip coupling of 10 dB loss (theoretically 2 dB). As the optical signal propagates through the silicon nitride low-loss waveguides (-0.3 dB), meets the TriPleX-InP interface with 5.5 dB loss (theoretically -3 dB), is split over 4 branches (-6 dB), enters the TriPleX again (-5.5 dB), is routed on TriPleX (-0.2 dB), interfaces to the InP (-5.5 dB), and recombines with the carrier (+3 dB). This results in a -36 Gain which is equal to 18 µA. Improvement of the fiber entrance losses (reduce

from 10dB to 2 dB) and InP-TriPleX interface losses (from 5.5 dB to 1 dB) is required to obtain 14.5 dB (1.97 mA) performance.

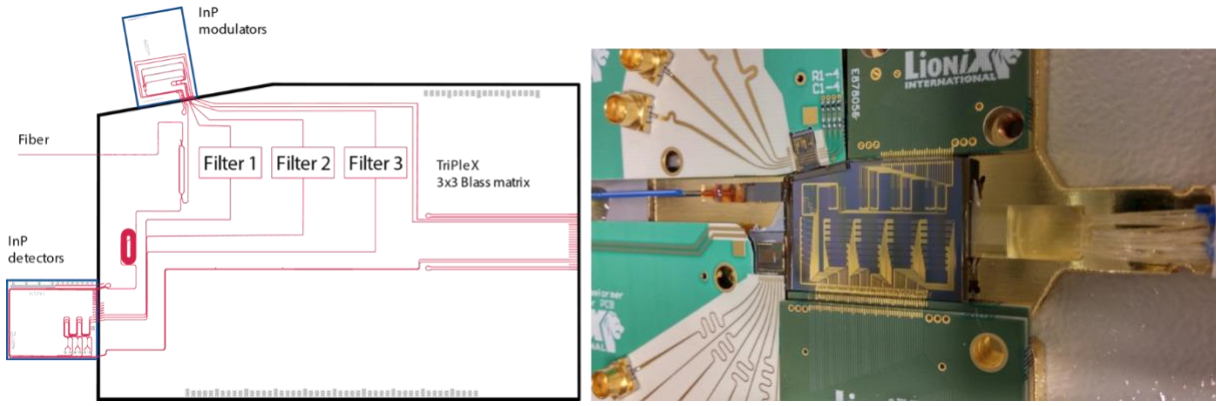


Figure 14. *Optical beamforming network architecture and assembly*

A challenge in this architecture is the **thermal management** of the assembly. The thermo-optic heaters on the TriPleX dissipate significant power which should, for each heater, remain localized on the chip. Therefore, a Peltier controller, or thermoelectric controller, is mounted directly underneath the basement of the chip-assembly.

A small sub-architecture of the OBFN, the laser cavity and adjustable mirror, is currently manufactured as hybrid laser. Record low linewidth (290 Hz) has been obtained over a tunable 80 nm in C-Band with 20 mW output power.

Optical Fiber Splicing

Fusion splicing was developed specifically to butt join optical fibers. Fusion splicers use an electric arc to weld two optical fibers together. The fusion splicing process uses localized heat to melt or fuse the ends of two optical fibers together. The process begins by preparing each fiber end for fusion. All protective coatings must be removed from the ends of each fiber. The fiber is then cleaved using the score-and-break method, usually with the aid of a tool or fixture. The quality of each fiber end is inspected using a microscope. The post joining attenuation of the fused joint is a direct function of the angles and quality of the two fiber-end faces.

The basic fusion-splicing apparatus consists of two fixtures on which the fibers are mounted with two electrodes. An inspection microscope assists in the placement of the prepared fiber ends into a fusion-splicing apparatus. The fibers are placed into the apparatus, aligned, and then fused together. Fusion-splicing usually utilizes electric arcs to heat the fiber ends causing them to fuse together. Arc fusion splicers can splice single fibers or 12- and 24-fiber-count ribbon fibers at the same time. The small size of the fusion splice and the development of automated fusion-splicing machines have made electric arc fusion one of the most popular splicing techniques in commercial applications. The splices offer sophisticated, computer-controlled alignment of fiber-optic cables to achieve losses as low as 0.02 dB. Fusion splicers more recently support splicing of polarization maintaining and multicore optical fibers performing automated rotation functions as well as fiber diameters from 80 μm up.

The picture to the right illustrates a conventional splicer. The detailed photo in **Figure 15**. shows the actual splicing platform. The red fibers being spliced can be seen coming into and leaving the splicing point.

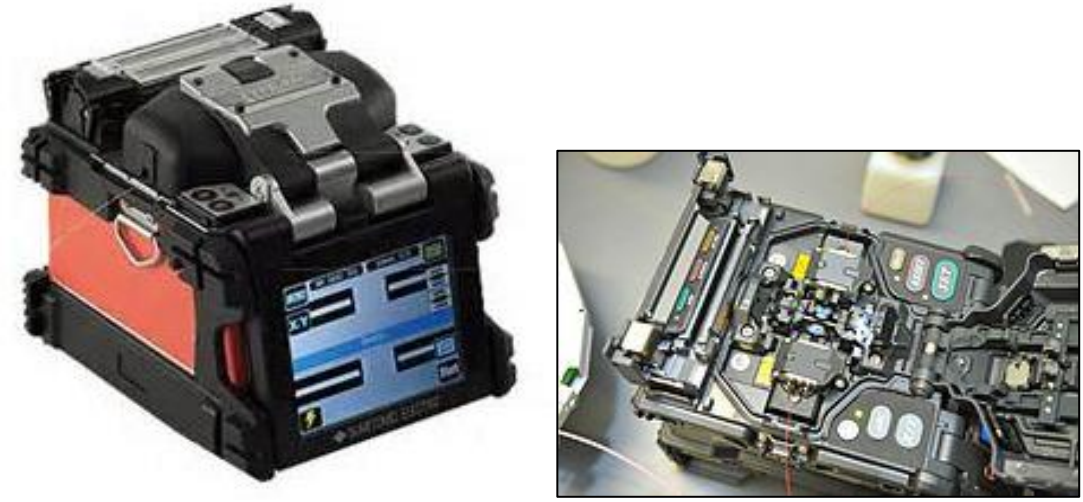


Figure 15. *Optical Fiber Splicer*

Laser Waveguide Formation

The graphics below are from the Yoo group at the University of California at Davis.

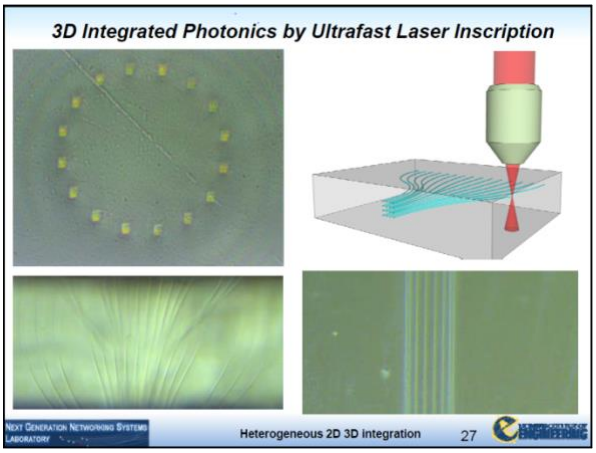


Figure 16. *Illustration of waveguides inscribed within a bulk solid utilizing femtosecond laser pulses.*

This graphic illustrates inscribing waveguides within a bulk solid utilizing femtosecond laser pulses. Through the use of fiducials, cameras, high accuracy stages, careful measurement of parts and some complex software, waveguides can be accurately located within a bulk solid and used to fabricate a waveguide from one known point to another. Alternately, the process can be used to fabricate waveguide structures that are difficult to make utilizing other methods. For example, a structure such as a linear to circular transition can easily be fabricated.

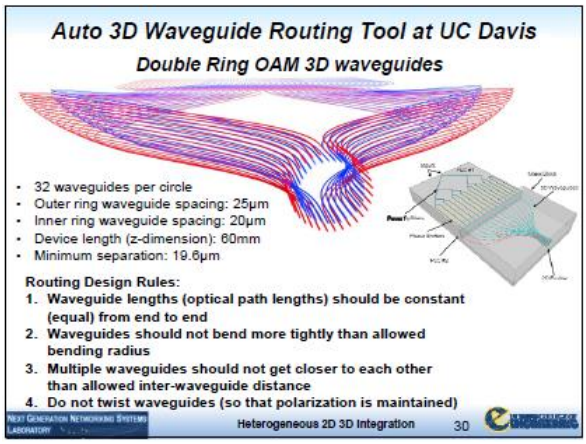


Figure 17. *Auto 3D waveguide routing tool at UC Davis*

The process works because the laser pulses increase the index of refraction enough to make a waveguide. An inscription rate of 150 mm/sec. has been demonstrated making the process potentially cost effective.

A similar process works in polymers and is being commercialized by several organizations including Vanguard Automation GmbH as described below. Laser generated waveguide is an emerging capability whose value and applicability are currently being assessed.

Vanguard Automation GmbH SONATA1000 SERIES

With its SONATA1000 series, Vanguard Automation offers the first industrial solution for in-situ printing of photonic wire bonds and facet-attached micro-optical elements. The system relies on high-resolution 3D multi-photon lithography and is geared towards printing of single-mode and multi-mode package-level connections.

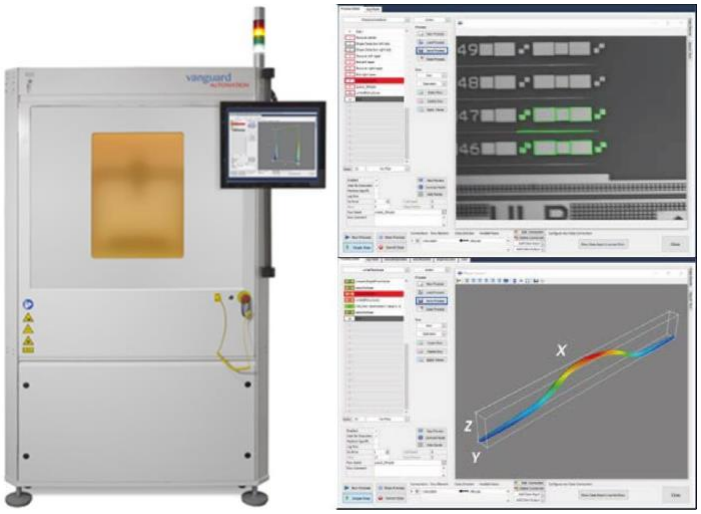


Figure 18. *Vanguard automation SONATA 1000 series*

Photonic wire bonds are single-mode freeform waveguides that efficiently connect integrated optical chips to each other or to optical fibers. The shape of the bonds is adapted exactly to the positions of the coupling interfaces, and high-precision alignment of the optical chips becomes obsolete. Moreover, by using tapered freeform waveguides, photonic wire bonding can cope with vastly different mode fields of the devices to be connected. The technique can be fully automated and is well suited for high-throughput mass production.

Using the same high-resolution additive 3D printing technology, the SONATA1000 enables also in situ printing of facet-attached beam-shaping elements. This approach allows precise adaptation of vastly dissimilar mode profiles and permits alignment tolerances compatible with cost-efficient passive assembly techniques.

Specifications and features:

- ≤ 100 nm on-chip placement accuracy of 3D-printed structures
- Up to 400 mm substrates possible
- Versatile machine concept allows coupling to various surface and edge emitting devices
- Software defined functionality and reconfigurability
- 3D waveguide routing
- Tailored process modules for coupling to customer-specific optical interfaces

The Silicon Optical Bench

This part fabrication concept was developed as a method to fill some high accuracy optical location requirements. The two figures directly below, **Figure 19.** and **Figure 20.**, show such a structure and some of the features that the optical bench concept enables. The optical bench concept depends heavily on a phenomena characteristic of <100> silicon wafers [4]. Specifically, some single crystal materials, including silicon, have etching rates dependent on the crystallographic orientation of the substrate. This is known as anisotropic etching. One of the most common examples is the etching of silicon in KOH (potassium hydroxide), where Si <111> planes etch approximately 100 times slower than other planes. Therefore, etching a rectangular hole in a (100)-Si wafer results in a pyramid shaped etch pit with 54.7° walls, instead of a hole with curved sidewalls as with isotropic etching.

The technique enables the fabrication of a variety of features with highly accurate locations because their locations are determined by semiconductor lithography. This example shows:

- "V" groove for location a fiber made with a long, rectangular aperture
- Square pyramid pit for locating a ball lens made with a square aperture
- Larger pit for a photo diode larger square aperture etch to a stop
- Conventional electrical conductors
- Potential attachment methods.

Utilization of the basic selective etch sensitivity allows many highly accurate structures to be fabricated.

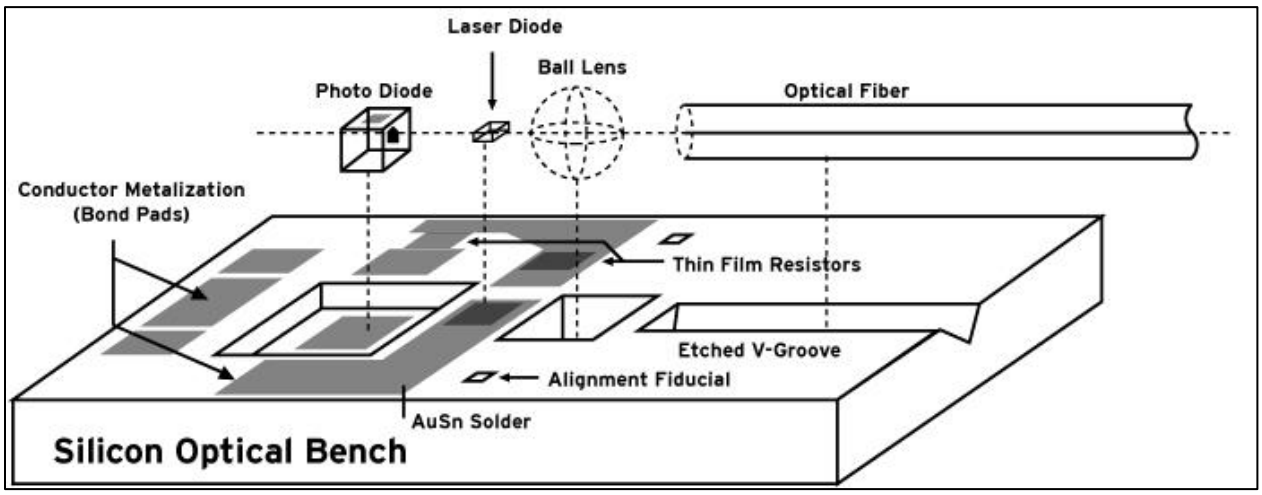


Figure 19. *Diagram of a silicon optical bench*

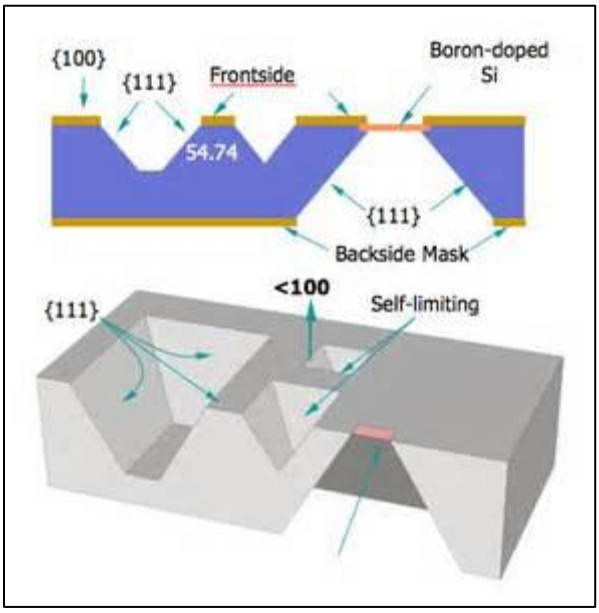


Figure 20. *Diagram of highly accurate anisotropic etching capabilities*

The next few figures illustrate some of the configurations that have been constructed utilizing this optical bench concept. These configurations usually incorporate more conventional assembly methods to complete the assembly process.

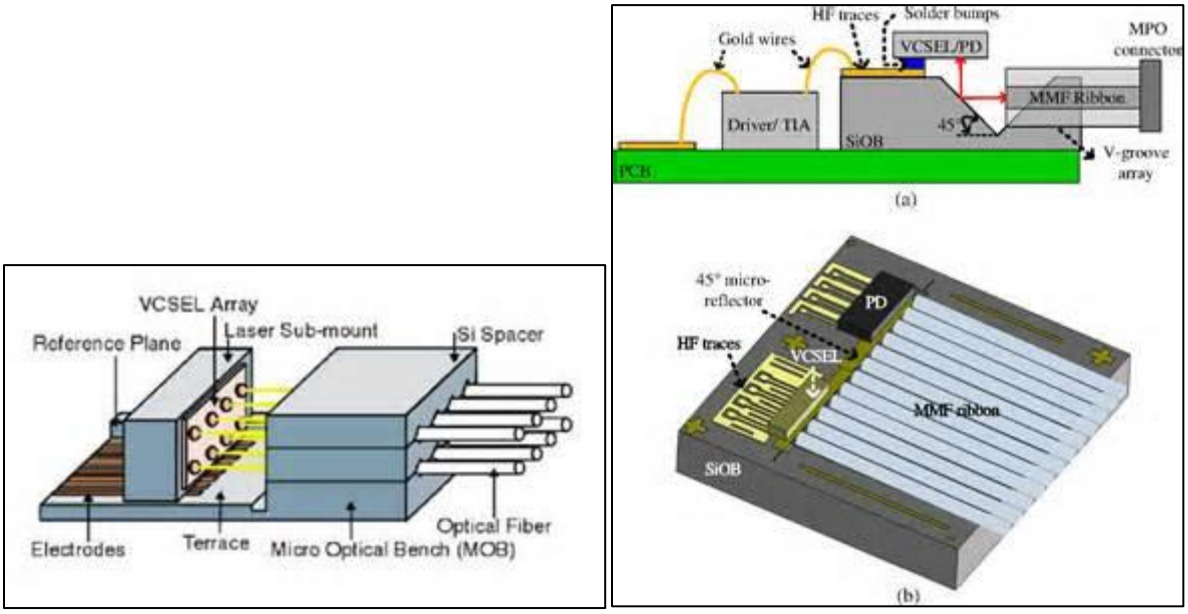


Figure 21. *Fiber alignment utilizing mechanical fiber butting & capillary action*

A paper by IBM researchers described a method of aligning fibers accurately utilizing capillary action as illustrated in the figure below from a talk given to the MIT CTR in April of 2015. This method is potentially important, especially if it is combined with capillary action to assist movement of the elements into position and hold them there while the joining method is affected by cooling of a solder, solidification of an epoxy or UV curing of an adhesive [5].

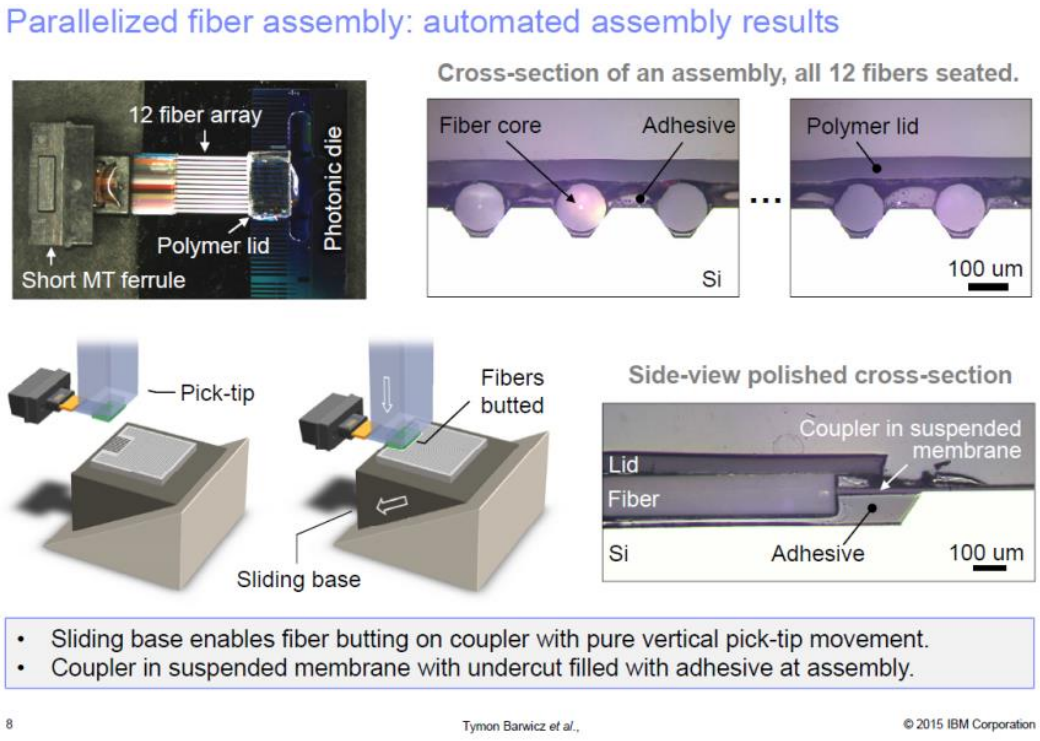


Figure 22. *Diagram of method utilizing capillary action for accurate fiber alignment*

Fiber Array Manufacturing

The market growth for PICs in combination with the required assembly accuracy is posing a challenge to obtain precise alignment of the fiber array at significant speed. Fiber arrays are a significant part of the bill of material of the assembly of a PIC in a package as fiber arrays are manufactured manually. An automated assembly tool is envisioned to fabricate arrays for 2, 4, 8, 16, 32 and eventually 64 fibers.

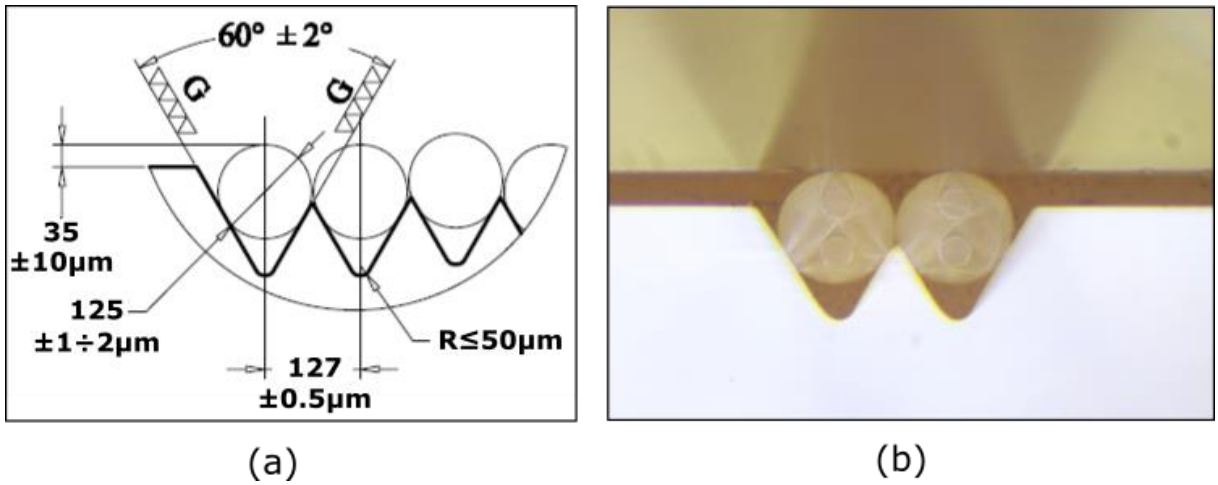


***Figure 23**. (a) V-grooves tolerance analysis, numbers may differ based on supplier and application. (b) Cross-sectional inspection of a 2-channels fiber array; orientation for vertical (TM) polarized light in fiber array.*

Dimensions are defined in **Figure 23.** Assembly throughput must be competitive. Feasibility of (semi-) automated assembly process on an industrial assembly platform capable of performing fine alignment in the far submicron range for fiber arrays.

Fiber Assembly, Chip-Fiber (Array) or Die-Fiber Assembly, Die-Die Attachment

The main challenge in photonic integration is to keep the light confined within the desired optical path, especially at an optical interconnect. High quality optical interconnect are designed and optimized for ***mode field matching***. Keeping the light confined in the optical path is a challenge for *interconnects on the chip* in the case of field stitching (large area photonic chip composed out of different masks/fields), or *interconnects of chip with another chip* (hybrid assembly/interconnect), or optical a planar interconnect (butt-coupling, or end face coupling) of ***waveguide to a fiber***. It requires careful 3D-alignment in both lateral (X and Y) and vertical (Z), the light propagation direction.

The alignment tolerance depends strongly on the mode field diameters of the fibers or waveguides that need to be aligned with respect to each other. A typical *telecom fiber operating at 1550 nm* has a Mode Field Diameter (MFD) which is in the order of 10 micron. Aligning such a fiber to another fiber or a waveguide, which is mode matched to the fiber mode, yields a tolerance of several microns when a coupling efficiency of ~ 65% is allowed (~2 dB misalignment loss).

When applications in the ***visible wavelength range*** are targeted, MFDs get smaller since they typically scale with wavelength. In the case of 3 µm MFDs, which is quite common for the wavelength range 400-700 nm, the alignment tolerance reduces to ~ 1 µm. In the case of *high-index-contrast waveguide technology*, such as SOI, InP or high contrast TriPleX, the on-chip MFDs are even smaller. In those cases, tolerances of 0.5 µm can already become quite dramatic. In the case of hybrid end-face coupling of such PICs, alignment accuracies and tolerances of only a few hundred nanometers can be tolerated.

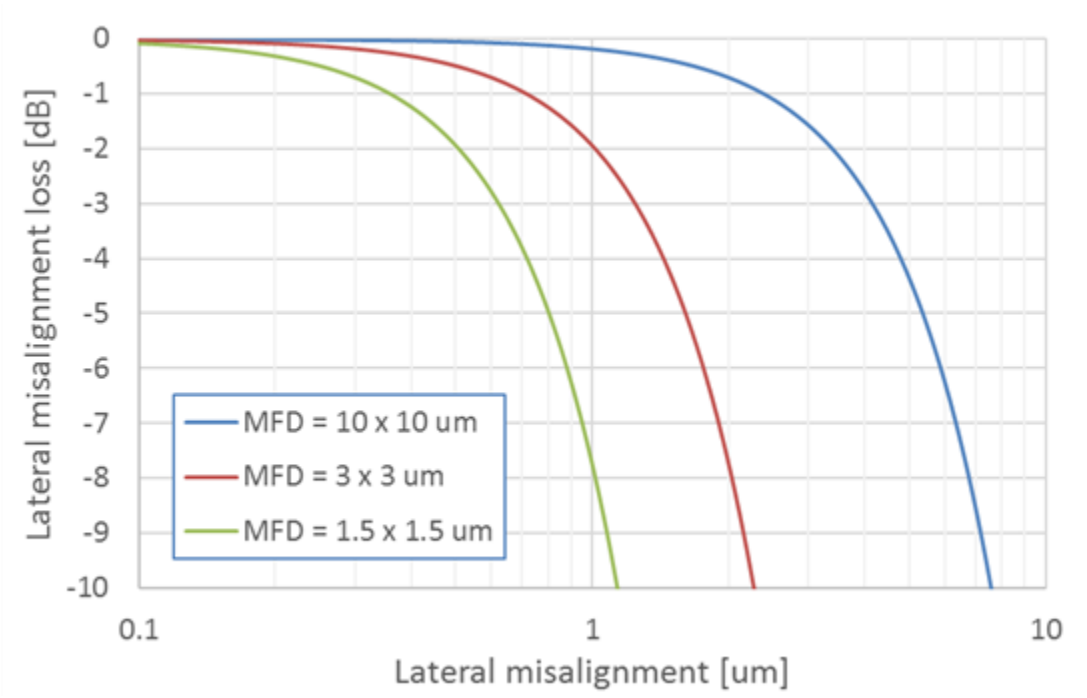


Figure 24. *Obtained optical losses related to relative lateral displacement for different mode-fields.*

An indication of the sensitivity and optical losses as function of lateral misalignment is calculated for different MFD and depicted in **Figure 24.**

Variation of interface losses as function of misalignment in the propagation distance of the light will effectively result in the introduction of a gap with different index and immediately result in unwanted reflections and interferences. This coupling challenge has been recognized since the development of the optical fiber by Corning in the late 60's where they showed their silica glass fiber with an attenuation of only 17 dB/km.

Interconnect challenges for fiber-interconnects and chip-to-chip-coupling are similar although the scale for chip-chip coupling accuracy is typically below 5 µm due to the small mode fields.

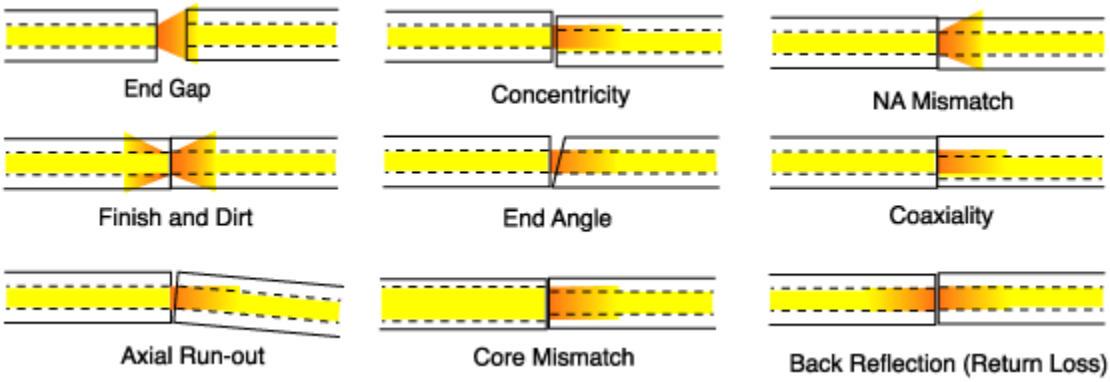


Figure 25. *Interconnect challenges and connector coupling loss [courtesy: Fiber Optic Connectors Basics, Styles, Trends]*

A solution to optimize the coupling and minimize the interface losses is to assemble tapered waveguides and tapered fibers that are mod-matched at the interface, as proposed in 2009 by Prof. Ron Reano and depicted in Error! R eference source not found. **26.** Measurements of fabricated devices demonstrate average coupling losses of 0.62 dB per connection for the TE mode and 0.50 dB per connection for the TM mode across the optical telecommunications C band (1530 nm – 1565 nm) using a silicon inverse width taper length of only 6.5 µm.

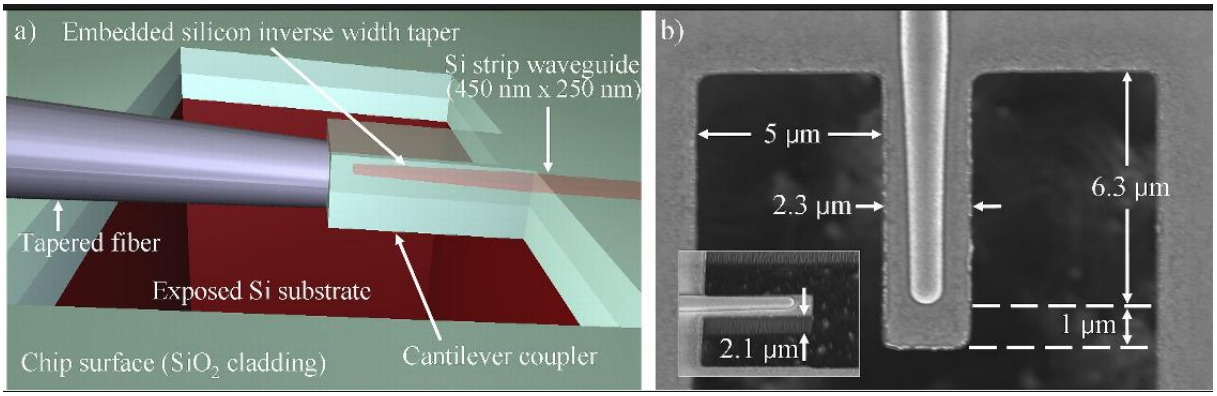


Figure 26. *Cantilever couplers for low-loss fiber-chip coupling [courtesy: Prof. Ron Reano, Associate Professor of Electrical and Computer Engineering, and ElectroScience Laboratory, of The Ohio State University].*

Planar Free Space Coupling of Waveguide to Photonic Circuit

An example of a free space coupled fiber-to-chip assembly is given by Kaiam. These very dense and high-performance multi-wavelength transceivers and modules meet the bandwidth requirements of today and tomorrow. Today, Kaiam manufactures their product in their 200 mm facility and uses a MRSI-705 and Palomar 3880s for automated alignment, bonding and assembly of the transceivers. Their MEMS based miniaturized optical bench provides robust, non-contact, fast and accurate, planar alignment solution as depicted in **Figure 27.**

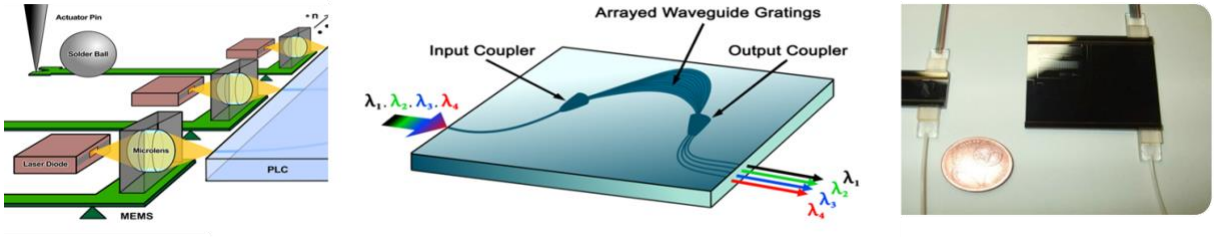


Figure 27. *Kaiam assembly strategy for high-volume production of AWGs and mux/demux modules.*

Product Enhancement Challenges:

Product enhancements and challenges for the first 5 years (2017-2022) are related to:

1. Ever growing capacity, from 10 G to 100 G to 400 G towards 1 Tb/s
2. New form factor interfaces such as Quad Small Form Factor Pluggable Double Density (QSFP-DD) (8 channels), and OSFP (both IEEE and MSA published standards for 400 G)
3. Tighter assembly tolerances
4. Lower power dissipation
5. The ability to operate under relaxed environmental conditions, humidity and temperature (15 ˚C – 55 ˚C).

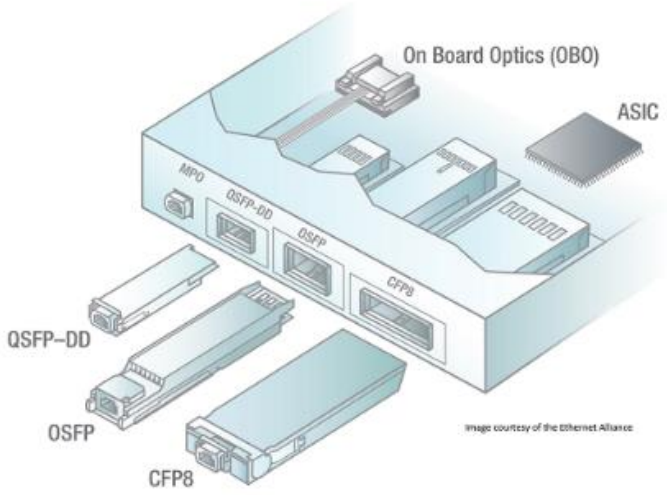


Figure 28. *Formfactor of transceivers and their envisioned interfaces.*

Currently the footprint of transceivers is dominated by electronics. The envisioned optics-electronics integration therefore focusses on:

1. Elimination of wirebonds
2. Introduction of RF capable carriers/substrates
3. Introduction of BGA/bumps/pads and flip-chip bonding processes
4. Fabrication of smaller electronics CDR/TIA/drivers/RF tracks
5. Introduction of automated submicron active alignment to meet the future assembly tolerances.

These activities require the following **functional building blocks or discrete components** to meet the transceiver product roadmap towards 2022:

- High-speed direct modulated lasers /modulators. (>50 Gbaud, short term 28 Gbaud/PAM4),
- Bandwidth increase: from 1270-1330 nm to 1270-1410 nm
- High speed detectors (>50 Gbaud, short term 28 Gbaud/PAM4)
- High temperature components for onboard optics.
- Redundancy for onboard optics.
- Integrated isolator on Photonic Lightwave Circuit (PLC)-PIC (optional)
- Higher density high speed RF lanes and approaches to get drivers and electronics (CDR/TIA) close to optics preferably using on chip tracks eliminating wirebonds where possible

Also thermal management is key for higher density of optics in given form factor.

Non-planar Coupling, Gratings and Mirrors

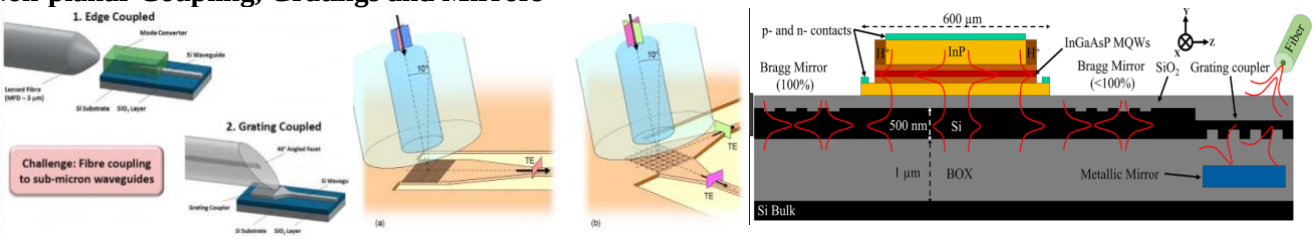


Figure 29*. Different strategies for using grating coupling for TE and TM polarization*

One of the biggest challenges of this integration is getting light on and off the PIC from optical fiber. For integrated photonics (both InP and Si) this is typically done either through edge couplers or grating couplers, as shown in **Figure 29.** Here fiber coupling from the photonic wire in SiPh [6].

The strategies developed by IMEC and Tyndall, and also used by IBM, are based on glancing coupling, entering the SOI chip 10 degrees from perpendicular incidence. The tricky (and costly) part comes in 'minding the gap' between the relatively large optical mode of fiber to the very small optical mode of a SOI on-chip waveguide. To put this into perspective, the diameter of a SM lensed telecom fiber for 1550 nm light is ~3 µm. This must be matched up to a SOI-waveguide mode with dimensions of ~ 220 nm x 450 nm. That's an area difference of almost 2 orders of magnitude (~7 million nm^2 vs 99,000 nm^2). A standard grating coupler in 220 nm SOI is -3 dB which equates to a 50% reduction in the transmitted power. This feature is particularly suited for in-line on-wafer test of integrated photonics (test) circuits.

More challenging is that SOI waveguides typically only support TE-polarized modes of light and the light coming in from a fiber is usually unknown and unstable requiring a mode convertor to clean up the signal before entering the waveguide. The 1 dB alignment tolerance for a typical edge-coupler is submicron (~ ± 500 nm) requiring time consuming and expensive active alignment during packaging. Additionally, these couplers usually require laser-welding to secure the lensed-fiber to the PIC as epoxy bonding suffers from small alignment drifts that would not be tolerable at these dimensions.

In the same way as in SiPh (SOI) there has been different in/out coupling methods developed for InP membranes (IMOS technology). Among them, edge coupling, vertical coupling and different types of grating couplers. Grating couplers allow alignment-tolerant mode matching from the compact photonic wires to a fiber and can be placed in high density anywhere on a chip. For applications like on-wafer testing or optical interconnect systems [7, 8], chip-to-fiber couplers with high efficiency, broad spectral response, and high fabrication yield are essential. In 2015 researchers at TU Eindhoven designed and developed a metal grating coupler for TE polarization useful for both InP and SiPh membrane platforms. The coupler consists of a metal grating, formed with buried stripes patterned in SiO_x and a metal mirror layer as shown in **Figure 30.** This type of grating coupler can be tuned by changing the properties of the grating; however, it was demonstrated for data-com and tele-com at 1550 nm wavelength. The grating adiabatically couples the photonic waveguide (400 nm x 300 nm) to a SM fiber (9 µm diameter). For assembly techniques of PICs on data-com tele-com, interconnects etc. high coupling efficiency is greatly needed. This type of metal grating combines a very high coupling efficiency up to 70% to a SM fiber placed at 10 deg and 10 µm vertical distance from the grating. The design also benefits from the use of well know basic fabrication process steps [9]. Due to the mode matching of the grating and SM fiber the alignment is more relaxed; allowing for automatic testing; however, freedom of placement of the gratings should be controlled to make efficient on-wafer testing.

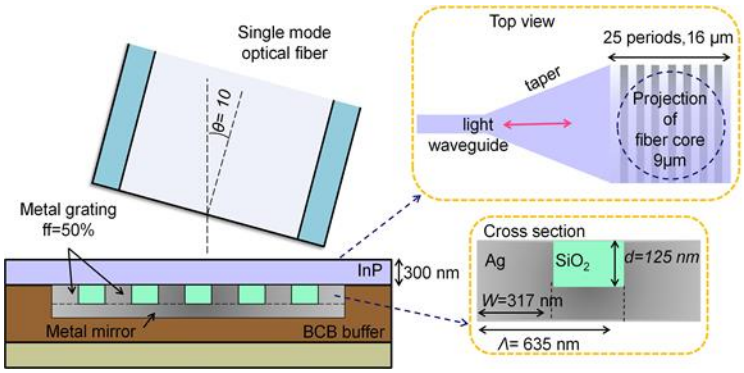


Figure 30. *Schematic of the buried metal grating. Insets show the tapered region from the waveguide towards the grating and the dimension of the indentations*

Accurate high-volume manufacturing is required to eventually serve market demand of millions of integrated components for telecom and datacom applications. This requires automation strategies for assembly and packaging that can meet the desired cost levels.

Manufacturing Equipment

The joining methods reviewed in previous section, require equipment to implement the alignment and attachment processes. Assembly, and thus equipment needs, depends on the component and package designs. The packaging chapter discusses design strategies that allow less accurate and more commercially available equipment for assembly. However, many assembly steps still require submicron alignments today.

Electronic manufacturing equipment is generally the starting point when seeking assembly methods for optical devices. That said, electronic assembly equipment tends to lack several characteristics important for optical assembly;

1. Alignment tolerance control required for optical coupling in X, Y, Z, T_x, T_y, and T_z.
2. Emphasizes assembly of planar structures, such as die on a substrate, vs assembly of non-planar structures such as lenses, fibers, and fiber arrays that optics sometimes requires.
3. High level of flexibility for zero or extremely low cost change-overs for concurrent manufacturing of multi-generations of photonics products driven by hyper scale data center applications. Electronic manufacturing equipment is usually configured for a specific application and not changed. Due to the extremely high volume of electronic devices, this equipment does not require flexibility. On the other hand, the high uncertainty of data center forecasts for increasing volume combined with high mix demands a new breed of assembly equipment that has high flexibility, speed and precision.
4. "Gentle" assembly for photonic devices made with III-V materials such as GaAs and InP. These are far more fragile than silicon materials commonly used for electronics. Most of the electronic assembly equipment does not need to have a very fine control of force applied to parts; photonics assembly equipment needs that.

Those limits aside, electronic equipment is attractive due to the low costs attainable when it is suitable. Electronic assembly equipment is built in relatively high volume, is widely available and typically has high assembly rates (10,000 ± parts/hr.). Thus, many optical assembly processes utilize conventional electronic assembly equipment and processes that may be modified to enhance its suitability for optical device assembly.

Manufacturers now make equipment that is able to place parts with an accuracy of 0.5 microns or smaller. In **Table 11.**, there is a summary of the capabilities and in Appendix B there are figures which illustrate some of the equipment available. The price of this equipment ranges from less than $100,000 to greater than $750,000 depending on the supplier, the capability, the assembly rate and the options selected. Most equipment is custom built to the buyer specifications for high volume applications.

The table is a simple summary of the six examples of commercially available high accuracy placement equipment that follows. Typically the equipment manufacturers measure the throughput as the time for a die bonding machine to pick-and-place a die onto a carrier with the target accuracy. Additional process time is required to complete the joint between the die and the substrate and is determined mainly by the product and process design and will add to the overall cycle time. The challenges result from the lack of common standards and specifications for precision, cycle time, and process yield among equipment suppliers. Often users find that these parameters cannot be achieved repeatedly in a high volume manufacturing environment.

In order to achieve certain levels of high accuracy, e.g., 1.0 μm or better, a special optical alignment unit is typically deployed between the pick-and-place period, which should be included in the pick-and-place throughput figure. The field optical alignment needs alignment fiducials on the die and the carrier, and sometimes on pick-and-place

tools. Those fiducials need to be high quality optically and high precision dimensionally in order to achieve high accuracy - similar to the requirement in semiconductor wafer level lithography processing.

Table 11. Overview of available assembly equipment. (Full data-sheets in Appendix C)

Supplier, Model	Placement Accuracy (microns)	Placement Rate (UPH)	URL
Semiconductor Equipment Corporation, SEC 850	±1.0	~60	www.semicorp.com
Finetech, femto2	±0.5	300	www.finetechusa.com
MRSI, MRSI-HVM1	±1.0	600	www.mrsisystems.com
Palomar, 6532 HP Die Bonder	±1.5	1,200	www.PalomarTechnologies.com
K & S, APAMA (TCB)	±1.0	<3,000	www.kns.com
ASM / AMRICA Nano	±0.3	~200	amicra.com
Frunhofer Flexible Assembly Cell	±0.25	360	
Ficontec Assembly Line Machine	Custom	Custom	www.ficontec.com
Suss Microtec XBS200 Wafer / Wafer			www.suss.com

The K & S APAMA, differs from the other four in that it is specifically designed and used for a process called Thermocompression bonding in which solder capped copper pillars with a pitch less than 60 microns are bonded utilizing an in-situ heating and cooling process to make joints utilizing solder and sometimes underfills. This process is intended for use with high density, high I/O (greater than 1000) contact devices such as microprocessors, ASICS and some memory devices. The force available to "squash pillars and solder caps to bring these points to be joined into contact over the typically relatively large area (25 mm x 25 mm) is up to 300 Newtons (~ 66 #s). While most optical devices do not have these high I/O counts, some proposed devices such as optical interposers may in the near future.

There are also a number of suppliers who focus on optical alignment and attachment of fibers, fiber arrays, waveguide arrays, lenses, lens arrays, and other optical components using passive or active alignment techniques.

Quality/Reliability

The quality and reliability requirements for optical devices are comparable to those for other products, especially electronic devices. Optical data communication products typically have a lifetime of 10 years or less. While some optical data communication products are still built to the Telcordia 40 year standard, most products, even those used in communication, do not need to be qualified to that standard.

These optical products, materials and processes, especially those utilizing new materials, processes, components and technology, do need to undergo rigorous qualification testing. Ideally, each of the new processes and materials will be carefully evaluated and qualified to ensure they will perform over an extended lifetime in the environment and under the conditions they may encounter.

Environmental Issues and Technology

Concerns have been raised concerning the use of some elements in optical devices. Lead in conventional solder must be excluded and leadfree alloys utilized. Concerns have been raised about arsenic and nickel with some efforts underway to exclude these elements from commercial products. Cadmium, lead and mercury, of course are currently banned from new products under the RoHS requirements.

Most optical devices do not utilize undesirable organics that are the subject of much of the current and emerging REACH requirements. These compounds are most likely to be found in optical devices used to do analysis where the compound interacts with some aspect/material/organism in the environment and generates a signal that optical technology is able to detect (we may be faced with the dilemma of utilizing detrimental compounds to detect other undesirable compounds).

The WEEE requirements related to recycling and disassembly have impacted optical products in only a minimal way to date. As optical devices proliferate, especially if they incorporate materials or elements that are viewed as detrimental, they will be scrutinized. Excluding these materials in new designs may forestall regulator issues in the future.

Finally, the Conflict Materials Requirements of the US SEC require publicly traded US companies to report the consumption of conflict materials, materials like gold, tin and tantalum, which come from certain parts of Africa. Thus, customers are asking suppliers to verify that the materials used in the products they buy do not contain materials from these sources.

Test, Inspection, Measurement (TIM)

Reliability and stability over the lifetime of the components requires an upfront detailed evaluation of interfaces, connectors and the PIC-basement properties that is used for the assembly, for example the expected temperature of operation of the PIC and the dissipated heat determine the desired temperature conductance of the material, the expansion coefficient of the PIC material induces stress and strain, that preferably closely matches that of the materials of choice.

CONTRIBUTORS

Table 12. Contributors including Participants in Santa Clara and Cambridge Workshops	
Paul van Dijk	LioniX International, The Netherlands
Robert Pfahl	iNEMI, USA
Graham Reed	U. Of Southampton, UK
Dan Evans	Palomar Technologies, USA
Meint Smit	Technical University of Eindhoven, The Netherlands
Richard Otte	Promex Industries Inc., USA
Ruud Steenwelle	Fraunhofer Project Center at the University of Twente, The Netherlands
Aura Higuera Rodriguez	Technical University Eindhoven, The Netherlands
Yi Qian	MRSI systems, USA
Henk Bulthuis	Kaiam, United Kingdom
Sonia Garcia Blanco	University Twente, The Netherlands
Bill Bottoms	3MTS, USA
Lionel Kimerling	MIT, USA
Ronald Dekker	LioniX International, The Netherlands
Huub Ambrosius	Technical University of Eindhoven, The Netherlands
Neil O'Brien	Finetech, USA
John MacWilliams	Consultant, USA
Sylvester Latkowski	Technical University of Eindhoven, The Netherlands

APPENDIX B - GENERALIZED HOOKE'S LAW

Axial Strain:

$$\varepsilon_x = \frac{1}{E}\left[\sigma_x - \nu\left(\sigma_y + \sigma_z\right)\right] + \alpha\Delta T$$

$$\varepsilon_z = \frac{1}{E}\left[\sigma_z - \nu\left(\sigma_x + \sigma_y\right)\right] + \alpha\Delta T$$

Shear Strain:

$$\gamma_{xy} = \frac{\tau_{xy}}{G}$$

$$\gamma_{yz} = \frac{\tau_{yz}}{G}$$

$$\gamma_{zx} = \frac{\tau_{zx}}{G}$$

$$G = \frac{E}{2(1-\nu)}$$

Where:
ε = Strain
γ = Shear Strain
σ = Stress
τ = Shear Stress
E = Young's Modulus
G = Shear Modulus
ν = Poisson's Ratio
α = Coefficient of Thermal Expansion
T = Temperature

*Stress and strain can have negative and/or positive values to represent tension and/or compression.

APPENDIX C – MANUFACTURING EQUIPMENT

Semiconductor Equipment Corp. (www.semicorp.com)

Figure 31. *SEC 860*

SEC 860 Specifications

- High accuracy, within 1-2 microns
- Custom systems for your specific application
- Fast and easy set-up
- Compact footprint
- Intuitive Windows based operating system
- Low maintenance with minimal calibrations
- Select only the options you need

MRSI Systems / Mycronic (www.mrsisystems.com)

Flexible, High Speed, High Precision for true multi-chip, multi-process, and multi-product high volume manufacturing

Figure 32. *Palomar's MRSI-HVM1; MRSI-HVM3*

Table 13. Flexible, high speed, high precision die bonders by MRSI Systems	
Placement accuracy (@±3 sigma @ 360˚ rotation)	<1 μm (HVM1)
	<2 μm (HVM3) (<1μm without tip rotation)
Placement cycle rate (total process time is application dependent)	600 UPH at <1 μm (HVM1)
	1200 UPH at <2 μm (HVM3)
Die dimension	~140 μm or larger
Die thickness	~50 μm or thicker
Repeatability	<0.1 μm (HVM1); <1 μm (HVM3)
Motion resolution	50nm (X, Y, and Z)
Angular resolution	0.00045˚
Z axis place to force or height with real time closed-loop control	Programmable force 10g to 5Kg Optional force 500g to 50Kg
Applications	Discrete devices (lasers, modulators, photodetectors, sensors, MEMS, LEDs, RF), Hybrid-integrated devices, Silicon photonics
Processes	Chip-on-carrier, chip-on-board, active optical cable, gold box, 3D stacking, pillar-to-pillar bonding, co-planarity bonding, flip-chip bonding, wafer level packaging
Configurations	Die attaching, flip-chip tools, co-planarity assembly, top heated head optional.
	Eutectic bonding, Epoxy stamping, UV epoxy dispensing and in-situ curing.
	Dies can be picked from Gel-Paks, Waffle-Packs, wafers, and tapes & reels.
	Automatic system conveyor handles boards, fixture trays, boats, and lead frames.
	Automatic wafer loading and unloading from cassette for multiple wafer handling. Wafer processing includes wafer mapping and ink dot detection.

Palomar (www.PalomarTechnologies.com)

Palomar Technologies (www.palomartechnologies.com)
6532HP Die Bonder - 1.5 Micron Die Bonder for Photonics Devices

Overview	Exceptionally accurate, high performance die bonder designed for the precise and high volume device assembly requirements of the photonic market.
Placement Accuracy	1.5µm, 3σ for ultra-precise device placement
Pattern Recognition	Palomar VisionPilot® with Radar Referencing® vision system
Placement Cycle Time	Up to 1200 UPH
Applications	• Photonics packages: VCSEL modules, QSFP packages, edge-emitting lasers, sensors, LiDAR • Silicon photonics modules • Ultra-fine pitch hybrid assemblies in Gold box • MEMS components
Performance	Motion Systems - 4-axis positioning system • XY Air Bearing Table with 0.1µm resolution • Z Axis with 0.2µm resolution • Tool Turrets - 6-position tool turret and 8-position bi-direction tool turret • Theta with 0-400 degree rotation and 0.000225 degree resolution
	Dies can be picked from Gel Paks, waffle packs, wafers and tape reel.
	Highly configurable allows multiple functions to be performed on a single system: eutectic bonding, epoxy stamping, UV epoxy dispensing and in-situ curing
Processes	Laser-to-submount, laser submount assembly to PCB, Gold box, wafer-level packaging, flip chip
Patent	Double-pick process protected under US Patent 6,776,327

Figure 33. *Palomar's 6532HP Die Bonder*

K&S (www.kns.com)

APAMA Plus

APAMA Plus

Process Requirements	Specification
Thin die handling (TSV 10:1) Die thickness	≥ 30 um
Fine pitch Cu Pillars Accuracy	± 1.5µ, ±20 mdeg, (3σ) ±1.0µ, ±10 mdeg, glass die (3σ)
Cu Pillar Stacking Planarity	2µ / 10mm
Bondhead Size	26x26mm
High force capability	3 to 500N
Process Control Force Accuracy	0.25N or 1% (whichever larger)
Bond Line Thickness Z-Height Resolution	± 1.0µ (with temperature compensation)
Low COO – Productivity	Heat Ramp: 350 C/s
	Cool Rate: 150 C/s
	Dry Cycle: <1.3 sec
Yield and Metrology	Die crack detection Contamination inspection Post bond overlay

Figure 34. *K & S APAMA Plus with specifications*

ASM AMICRA (amicra.com)

NANO – 0.3µm Technology Leading System

Figure 35. *ASM AMICRA's NANO Die Bonder and Flip-Chip Bonder*

NANO Specifications:

- UPH: Up to 200

- Placement Accuracy: ±0.3 micron, 3 sigma, ultra-high accuracy die attach/ flip-chip system for eutectic and adhesive placements, cycle time of ~ 15 sec.

- Multiple options: Dynamic aliment, flip-chip unit, dispensing system, UV-curing unit, contactless laser heating unit for up to 500 °C, pulse heating unit for up to 450 °C, heated pick up tools for up to 350 °C, wafer mapping, single component tracking, post bond inspection. Chip-to-wafer and chip-to-chip capability. Bond force up to 2 kg.

- Large working area with up to 330x300 mm

Finetech (www.finetechusa.com)

Figure 36. *Finetech's FINEPLACER femto 2*

FINEPLACER® femto 2 is a fully-automated die bonder with a placement accuracy of 0.5 µm @ 3 sigma offering flexibility for prototyping & production environments.

Fully protected from external influences, the system stands for highly stable assembly processes with the focus on maximum yield.

Combined with a refined pattern recognition, this all-new Vision Alignment System opens up a new dimension of application flexibility and accuracy. IPM Command, the fully revamped FINEPLACER® operating software, supports a consistent, ergonomic and clearly structured process development.

Specifications:

- Placement accuracy of 0.5 µm @ 3 Sigma on small to large substrates
- Wide range bonding force control
- Operating software with full process access and intuitive programming
- Safe and controlled process environment with cleanroom quality
- Fully automatic and manual operation
- Numerous bonding technologies (adhesive, soldering, thermocompression, ultrasonic)
- Full process traceability and protocol function incl. photo capturing
- Plug & Play configuration of process modules

Application Assembly Examples:

- Laser diode
- Laser diode bar
- Micro-optical bench
- VCSEL/photo diode (array)
- Optical sub assembly (TOSA/ROSA)
- Flip-chip bonding (face down)
- Precision die bonding (face up)

Ficontec (www.ficontec.com)

Figure 37. *The A1200 assemblyline machine system*

A general purpose high accuracy machine or process building blocks or series of machines are customized to customer needs.

- customized solutions for automated micro-assembly, packaging and testing of photonics-based components, micro-optic assemblies and opto-electronic devices.
- passive and/or active alignment and thermal or non-thermal assembly/bonding, or fully-featured optical test systems for full LIV testing as well as spectral and near/far-field beam characterization
- multiple in-line systems can be daisy-chained to encompass an entire process segment

Fraunhofer

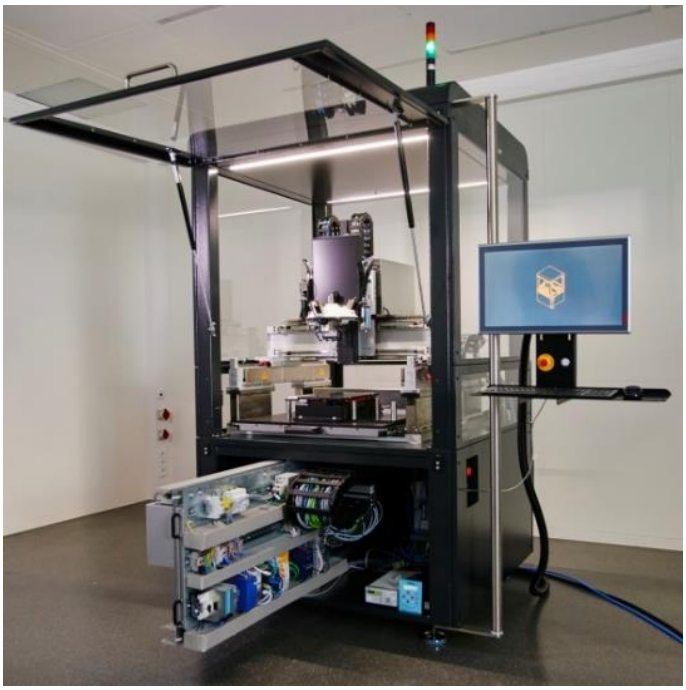


Figure 38. *Fraunhofer's flexible assembly cell*

Fraunhofer Flexible Assembly Cell Specifications:

- Up to 300 mm substrates
- Cycle time: 10 sec/piece
- 0.25 micron bonding accuracy
    - Die Attach Film
    - Soldering
    - Laser welding
    - UV curing
    - Dispensing on non-planar structures
- Test & inspection
- Die sorting and feeding
- Fully programmable
- Advanced manipulation capabilities
- Process development service
- Quick process interchange
- Good flexibility vs cost ratio

SUSS MircoTec (www.suss.com)

An example of a wafer-to-wafer bonding tool is the XBS200 made by Suss Microtec.

- Bonding force: 60 or 100 kN, repeatability: < 2 %
- Temperature: ≤ 550 °C, repeatability: < 1.5 %
- Pressure: 5x10-5 mbar – 3 bar
- Precise process recipe control for all bond parameters
- Ramp function
- Fast heating (40 K/min) and active cooling (40 K/min)

Figure 39. *Suss MicroTec's XBS200 wafer-to-wafer bonding tool*

APPENDIX D - SINGULATION METHODS

SAW SINGULATION

Historically, wafers are singulated using mechanical means such as scribe and break and sawing. Today scribe and break is used only for specialized applications. Saw is now the mainstream singulation technique that is able to accommodate new and diverse applications with high precision and high yields. The precision of state-of-the-art sawing is 1 micron both in X, Y and Z dimensions for cuts. Most of the remaining variation is from blade wear which can cause die sizes to increase from lot to lot. State-of-the-art saw machines can be programmed to catch blade KERF reduction so that the blades can be replaced.

Blades can be made as thin as 15 μm for low exposure (?), highly thinned wafers but such narrow kerfs are not viable on thicker wafers.

Blades consist of diamond embedded in nickel, in resin or in vitrified materials to provide the best capability for varied sawing applications. The myriad of available blades make saw singulation a very flexible wafer singulation process. In addition, blades can be made to order with side wall bevels and to fill novel sawing applications such as making needles or obelisk shapes on a substrate.

The main limiting factors for sawing are: (1) chipping of brittle materials and (2) vibration control while sawing smaller die to ensure the die do not "fly off". **Figure 40**. shows gouging and chip outs infringing into the active area of various brittle materials that are not difficult to saw.

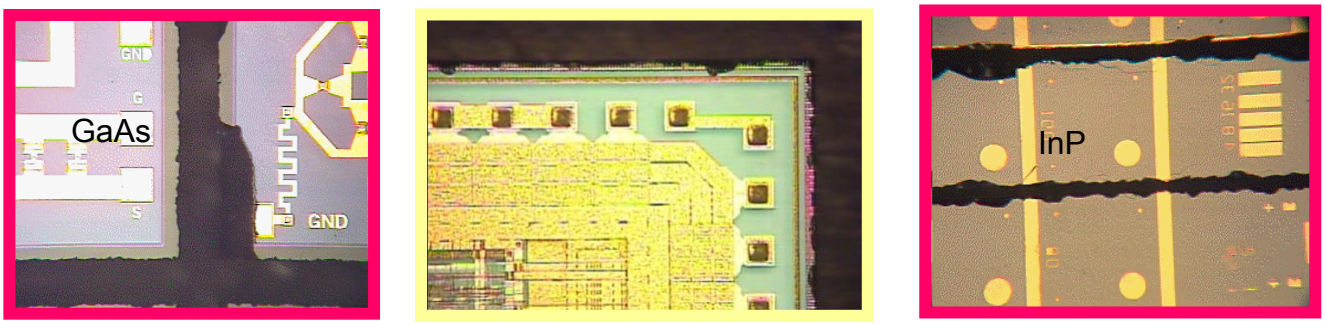


Figure 40. *Three examples of materials that are difficult to saw without chip outs.*

Small die, and die with high thickness to area ratio, are difficulty to grip firmly and keep in place during sawing resulting in chip outs and fly-offs. Yield loss due to the lack of adhesion of very small dies under high blade forces can be reduced by thinning wafers to ultrathin levels, and increasing the area to thickness ratio to greater than 2.

Sawing applications of sub - 0.3 mm and smaller die requires extensive sawing time on machines making a batch process more attractive. Batch singulation processes such as plasma etch or stretching are also very effective in reducing Kerf widths and increasing die counts per wafer.

LASER SINGULATION

Laser beam singulation processing is the main technology that has been developed to address the limitations of saw singulation. A handful of commercialized manufacturers build laser singulation equipment with Disco the leader. The graphic below illustrates the evolution of singulation methods including the role of laser singulation.

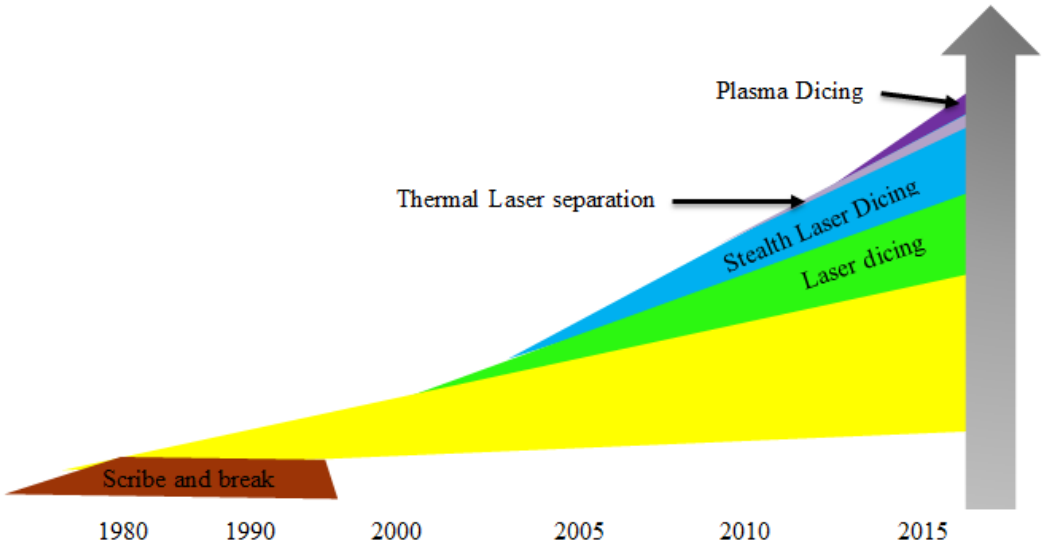


Figure 41. *Evolution of singulation methods*

The two main types of laser singulation and their general characteristics are illustrated in **Figure 42.** below.

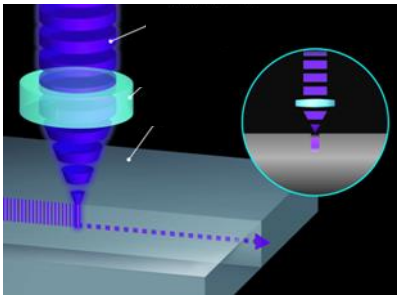
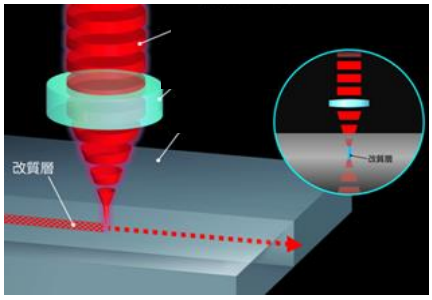
Technology	Thermal Ablation	Stealth Dicing (Internal processing)
Method	Sublimation by irradiating with a short pulse laser	Creating SD (modified) layer by focusing laser inside material
		
Process	Grooving, Scribing, Full cut, DAF cut	Chip separation by SD layer creation + Breaking/Expand

Figure 42. *The two main types of laser singulation.*

Thermal laser singulation, or laser ablation dicing as it is also called, is now widely used for dicing of sapphire, LEDs, GaAs, InP and other brittle wafers. Due to the limited depth of cut from a laser beam, multiple beam passes are needed depending on the wafer thickness and geometry. Ablation is rarely deployed for complete through cutting of a wafer. Laser trenching and grooving are performed in conjunction with other mechanical means reminiscent of

classic wafer scribe and break methods. Partial laser dicing or grooving from the top of a wafer is done while supporting the wafer with a dicing tape on a standard frame that is compatible with equipment for subsequent assembly. Singulation is completed by either stretched or roll broking the wafer while it is supported by a tape. A variety of tapes for various materials or dicing applications are available for these applications.

"Recast" (ablated material "blown out" of the kerf) by laser ablation contaminates the wafer surface. Modern laser machines are equipped with a pre-spin on coater and a post wafer washer to protect wafer surfaces from this ablated material.

Stealth laser dicing has rapidly gained wide acceptance as it does not require coating and is a contactless process which is ideal for MEMs devices. Stealth damaged zones are not on the surface but internal and thus away from active circuitry as shown in the photos of **Figure 43** Wafers can be laser beamed from the front side or backside as long as the streets are empty and have no features such as test bond pads. The singulation process can be customized by using multiple beam passes depending on the wafer type and die geometries. Streets can be designed to be as narrow as 10 µm with no limit on die size or even die shapes. Curved and multiple cornered dies can be formed by stealth laser and expand.

Stealth lasing is not a flexible technique as most wafers have to be designed from the start with no street features to ensure an even cut. Conventionally, device engineers have placed a myriad of wafer monitoring structures in the streets which is OK for saw singulation but a problem for laser singulation. Thus, it is important that wafer designers work closely with backend assembly personnel to maximize yield and minimize cost.

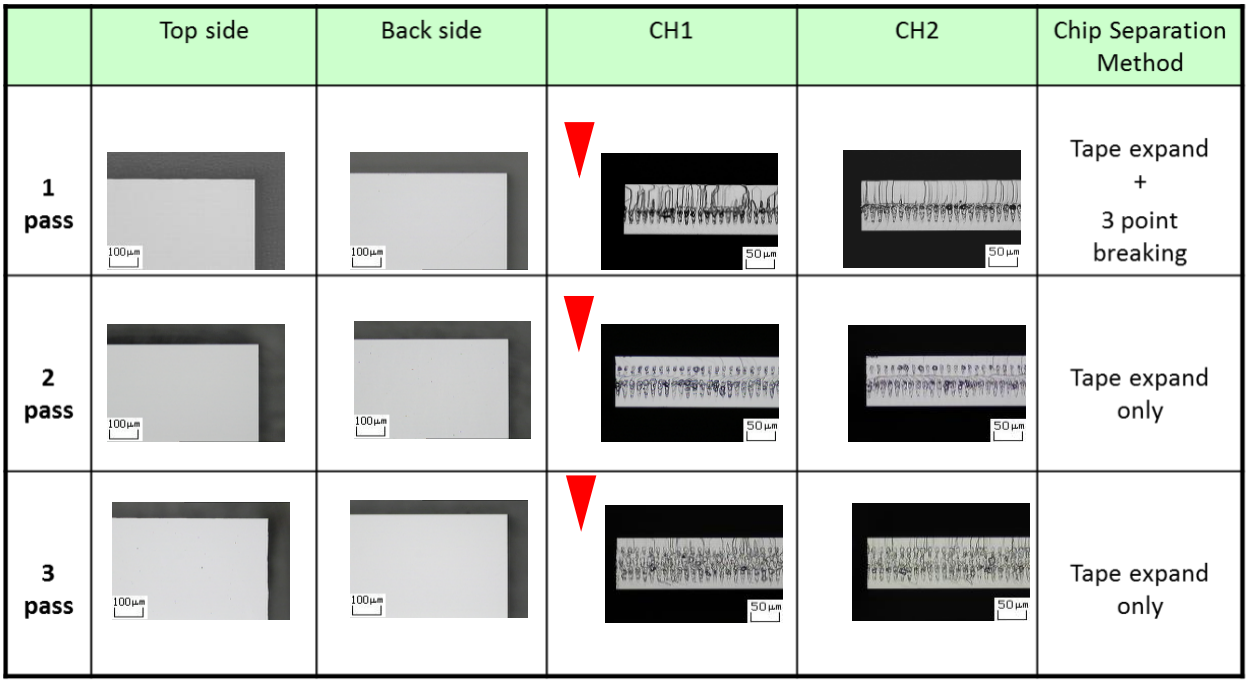


Figure 43. *Photos of die singulated with stealth dicing.*

Singulation utilizing stealth lasing requires stretching or rolling or grinding the wafer to induce complete fracture and/or die separation. As shown in **Figure 43.** the side walls are straight with no chipping. After a decade of development, stealth lasing has been implemented for the singulation of many types of III-V and II-VI wafer materials as shown in this chart by Disco.

Both ablation and stealth lasing techniques utilize expensive equipment and require high maintenance from highly skilled personnel compared to wafer saw dicing. Thus, for small volume and research work, saw dicing at the expense of yield loss and through put are commonly used as best as is possible.

Utilizing a laser on a product requires extensive customization and development of the process as lasers have to be tuned to the material to be processed. Laser beam effectiveness is very sensitive to surface and crystalline properties. Due to the long setup times on laser machines to accommodate a mix of wafer materials, laser systems are now often dedicated to one wafer material to eliminate set-up time and labor cost.

PLASMA ETCHING SINGULATION

A newer wafer singulation method that is emerging and in development utilizes plasma etching with SF_6 gas, an established foundry batch process. Plasma singulation reduces the cost of singulation when a wafer contains a large number (quarter million) small dies such as RFIDs or discretes because conventional wafer singulation would take a relatively long time even with a high speed laser. A benefit of the process is that plasma etched die have smooth edges as illustrated in **Figure 44.** and thus resist damage during subsequent handling and assembly. A further unique capability is the ability to make die any shape; they need no longer be only rectangular but round, hexagonal, etc. Like laser dicing, plasma etching is. another singulation method where wafer designers must work closely with the backend singulation personnel to ensure the kerf does not contain metal or other structures that will interfere with the silicon etching process. Another issue is that this process is not as established and is not "friendly" to the conventional dicing tape film frame that assembly equipment utilizes resulting in specialized handling fixtures.

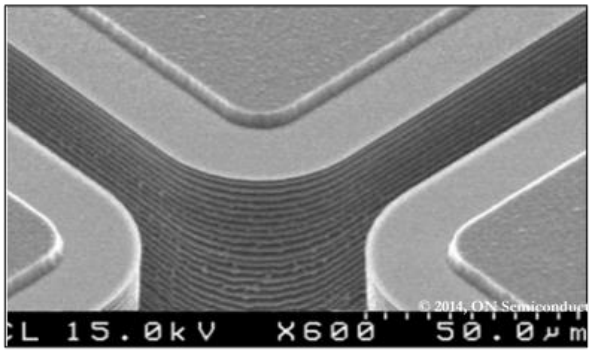


Figure 44. *Die edge and kerf resulting from plasma etch singulation.*

DICE BEFORE GRIND

Mixing changing the sequence or combing two or more singulation techniques is now widespread. The most common combination is "dice before grind" or DBG as illustrated in **Figure 45.**

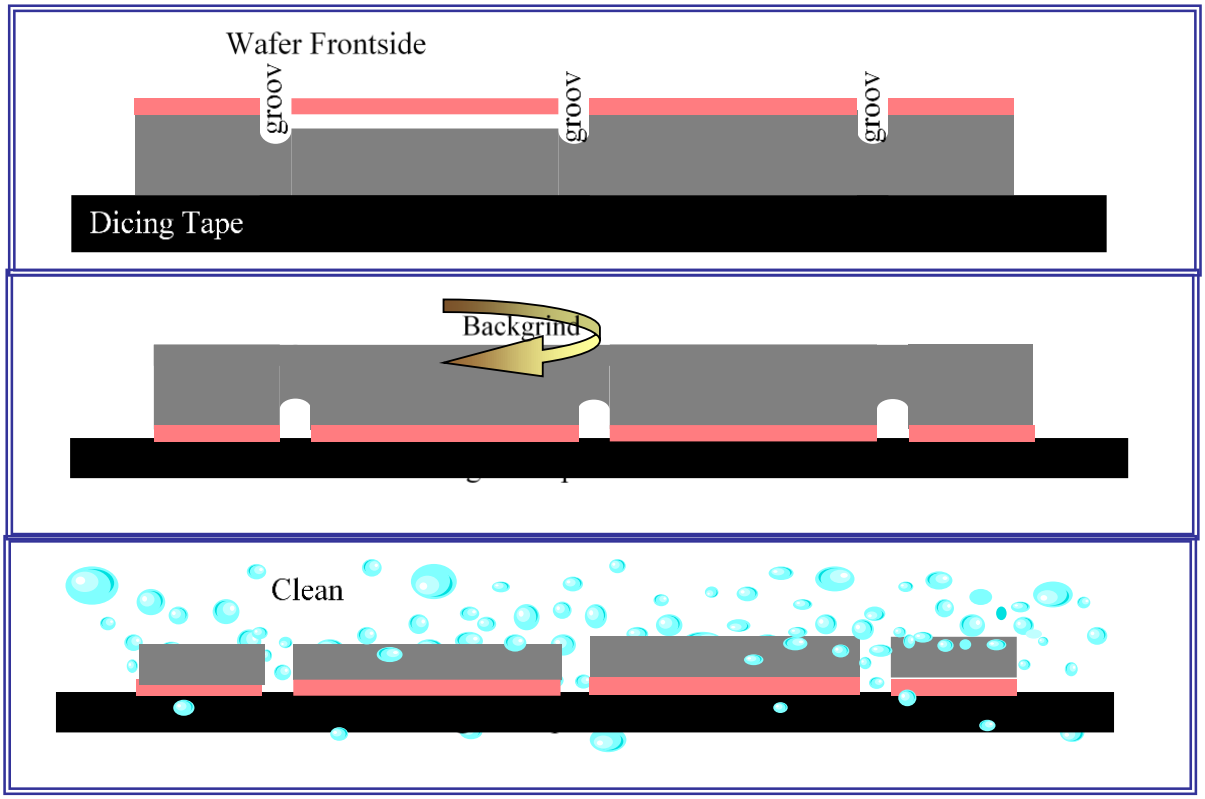


Figure 45. *Illustration of the dice before grind (DBG) singulation process.*

Dice before grind (DBG) involves grooving or trenching the topside of the wafer with a saw. The circuity side of the wafer is then taped with a grinding tape and the dicing tape on the back side is peeled off and to expose the wafer backside for grinding. Material is removed by grinding until the die are singulated but supported by the backgrind tape. The die must then be removed from the backgrind tape and "flipped" over for the die attach process.

Novel combinations of saw, laser, plasma, Dry etch, wet etch and grind are been pursued by the industry with to improve die strength and reduce cost. Some examples are shown in **Figure 46.**

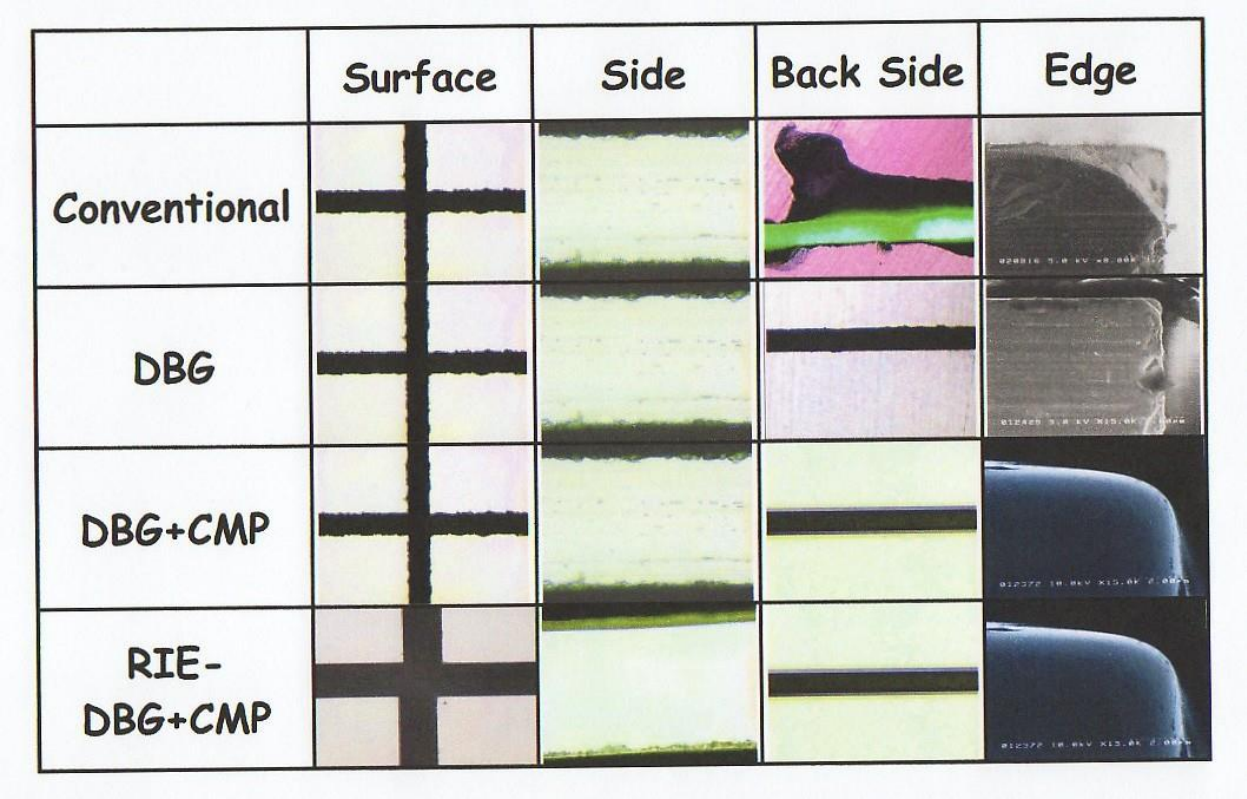


Figure 46. *Photos of die finishes from combinations of grinding and singulation methods.*

Figure 47. summarizes some of the combinations of thinning and singulation methods that are in use and under development for various purposes. Each has its pros and cons. The technical benefits, process development cost and resulting piece part cost must be considered and evaluated for specific applications and the resources available to implement the combination.

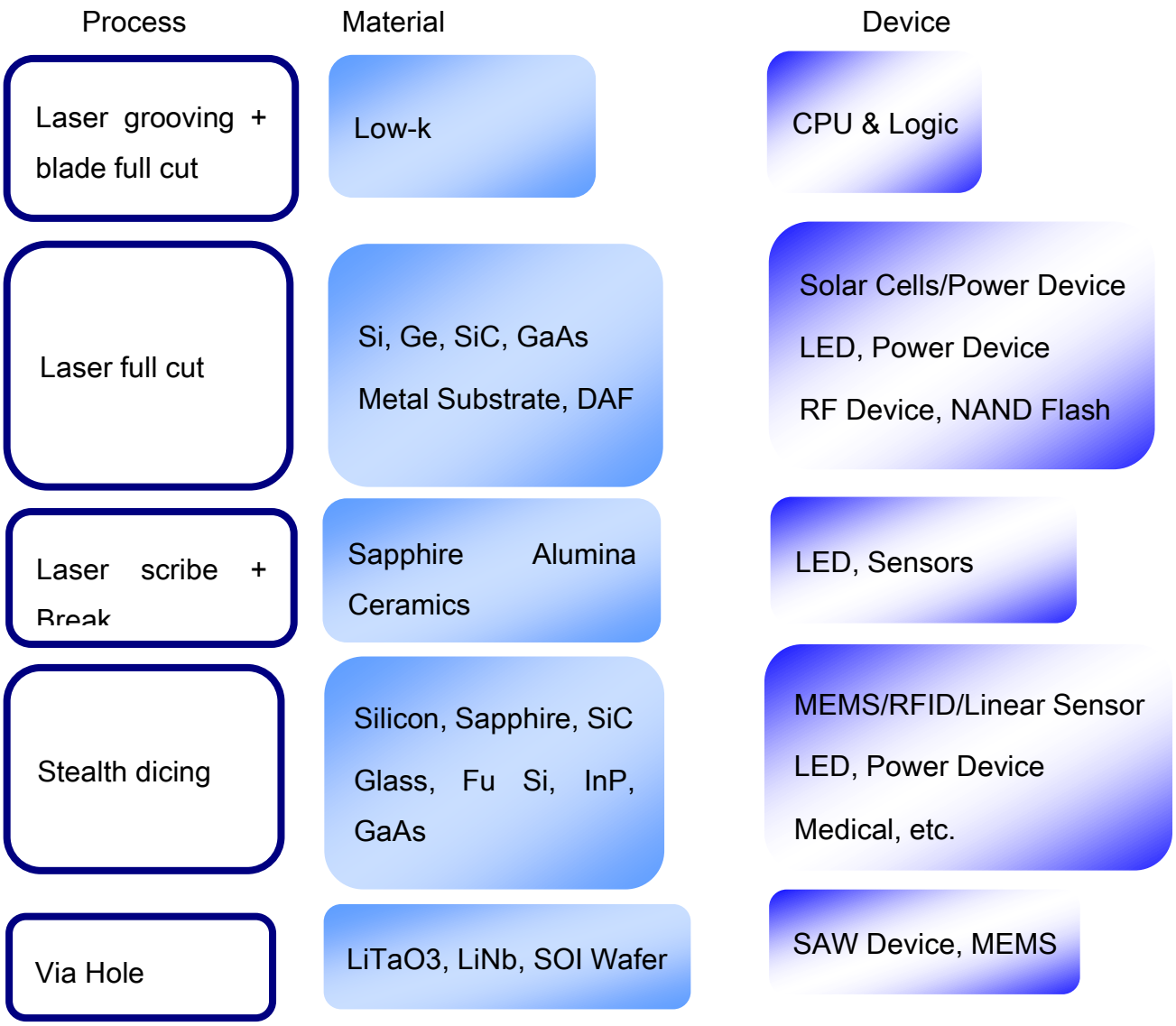


Figure 47. *Combinations of thinning and singulation processes, materials and devices in use or emerging for various materials and devices including optical applications.*

EDUCATION AND TRAINING

Assembly and Test are essentially manufacturing activities and thus require education and training in a series of disciplines and skills. The tables below provide some guidance on these needs.

Table 14. Academic Education Requirements

Knowledge Required	Content
Basics of materials	Properties of metals, polymers, ceramics. Properties are Young's modulus, Poisson's ratio, melting point, Tg, strength, ductility, etc.
Mechanics of Materials	Bending, thermal expansion, Hooke's General Law, thermal conductivity, corrosion, water absorption
Chemical and electrical properties of materials	Dielectric constant, loss tangent, effect of water, etc. solubility in water and common liquids, effect of UV and other environments on properties. Surface properties, adhesion, oxides, etc.
Processing of materials	Extrusion, rolling, casting, forging, injection molding, compression molding, transfer molding, etc.
Basic chemistry of organics	Epoxies, their structure, curing properties mechanical and chemical properties pre and post cure as well as their processing characteristics. Acrylates and their properties, both pre and post cure with UV and thermally. Also urethanes, silicones, liquid crystal polymers, etc.
Standard joining methods	Typical joining methods and their pros and cons; welding, soldering, adhesives including epoxies, acrylates. CiO2 to SiO2 bonding, plasma surface prep, etc. (Harman and Manko have good books on metal to metal bonding and soldering.)
AC/and DC electricity & electronics	Voltage, current, frequency, power, electronics, transformers, capacitors, inductors, transistors, ions, conductors, semiconductors, non-conductors
Maxwell's Equations in integral form	Relation to electricity, magnetism, radio signals, light signals, electromagnetic spectrum, properties vs frequency, interaction with matter vs frequency.
Signal transmission and processing	Modulation methods, signal processing, impulse response, propagation in free space, over conductors, through waveguides including fiber and in media in general.
Basic programming	Stored program concept, self-changing, iteration, solution seeking, etc.
Computer controlled equipment and microprocessors.	Computer control of machinery, networking, program storage, program management, etc.
Basics of Statistics	Gathering data, maintaining integrity, managing data bases, standard deviation, mean, median, Parato charts, statistical process control, control limits, Cp, Cpk, etc..
Measurements	Basics of mechanical, electrical, optical metrology.
Financial basics	Basic business financial concepts; revenue, costs, elements of cost, product cost elements, overhead, cash, AR, AP, depreciation, equity, etc. "The $ in must be greater than the $ out". "We make investments in order to make more money back utilizing the result of the investment," etc.

Table 15. Training Requirements	
Skill Require	**Areas of Training***
Personal Behavior	Show up on time. Be prepared to perform your job. (Be present mentally and not preoccupied with a non-job related issue, rested, healthy, properly dressed, etc.)
Safety	Rules, behavior, precautions, etc., related to safety for machinery, chemicals, slips and falls, people related, spills, MSDSs.
Quality	Follow the rules. Ensure procedures are followed. Go beyond the formal requirements and propose improvements. Follow the Japanese "5S" rules. Follow "Deming's 14 Rules For Management". Use statistics to improve yield and minimize variation.
Cost	Why cost is important, sources of cost, minimizing cost, proposing cost reductions, minimizing waste, maximizing reuse and recycling.
Equipment operation	Safe operation, machine setup, standard operations, maintaining records, impact of each process on cost, use of the operating manual, machine maintenance,
Metrology	Use of calipers, electronic and optical measurement methods, storage of data and analysis, ensuring accuracy, measuring joint strength.
Joining methods	Training in soldering, welding, adhesive application, pot life, mixing of epoxies, storage and handling of organics and other materials,
Interpreting Instructions	Read what it says, ask question, make sure you understand, do not "assume", eliminate and resolve ambiguities.
Completing Jobs On Time	Ensure you understand what is required, ensure all of the instructions, materials equipment and other resources are available. Start as soon as possible. Look for potential barriers ahead and ensue they are eliminated. Be prepared to revise your approach. Ask for help. When you error, admit you made a mistake, learn from it, ensure you do not make it again. Do not hide your errors.

*While training is often highly specific to each job, basics apply to all jobs.

REFERENCES

[1] G. Harman, *Wire Bonding in Microelectronics, Materials, Reliability, and Yield*, 2nd ed. San Francisco, CA: McGraw Hill, 1997, pp. 148, Table I-6.
[2] SUSS MicroTec. "Products & Solutions: Wafer Bonder." Internet: https://www.suss.com/en/products-solutions/wafer-bonder, [Oct. 5, 2020].
[3] C. Roeloffzen, L. Zhuang, C. Taddei, et al. "Silicon nitride microwave photonic circuits," *Opt. Express* Vol. 21, Issue 19, pp. 22937-22961, 2013.
[4] Wikipedia. "Etching (microfabrication)." Internet: https://en.wikipedia.org/wiki/Etching_(microfabrication), July 8, 2020 [Oct. 5, 2020].
[5] T. Barwicz, Y. Taira, T. W. Lichoulas, et al. IBM Presentation to the MIT CTR, Topic: "Photonic Packaging in High-Throughput Microelectronic Assembly Lines for Cost-Efficiency and Scalability." Massachusetts Institute of Technology, Cambridge, MA, April, 2015.
[6] D. Lockwood and L. Pavesi, *Silicon Photonics III: Systems and Applications*, Vol. 122. Berlin: Springer, 2016.
[7] J. Hofrichter, W. M. J. Green, F. Horst, et. al. "Grating couplers as optical probe pads in a standard CMOS process," in *8th IEEE International Conference on Group IV Photonics*, 2011, pp. 127–129.
[8] Y. Atsumi, T. Sifer, J. Kang, Y. Hayashi, N. Nishiyama, and S. Arai, "Ultraviolet-induced wavelength trimming of BCB-buried athermal Si slot wavelength filters," in *2013 Conference on Lasers and Electro-Optics Pacific Rim*, 2013, pp. 1–2.
[9] A. Higuera-Rodriguez, V. Dolores-Calzadilla, et al., "Realization of efficient metal grating couplers for membrane-based integrated photonics." *Optics Letters*, Vol. 40, Issue 12, pp. 2755, June 15, 2015.