ELECTRONIC-PHOTONIC DESIGN AUTOMATION

Contents

EXECUTIVE SUMMARY

The electronic design community is large and has years of experience with ever improving commercial design tools. The photonic design community is relatively small and until recently used "homegrown" design tools or commercial tools developed for experts and researchers. To tap into the larger traditional electronic IC design community using Electronic Design Automation (EDA) solutions, the goal should be to mimic the function of existing EDA platforms when incorporating the photonics aspects resulting in an Electronic Photonic Design Automation (EPDA) environment.

The introduction of Process Design Kits (PDKs) in 2008 together with the Multi Project Wafer (MPW) runs has largely supported the more widely application of PIC technology in domains outside of the traditional telecom space and accelerated the transition from academic research into commercial manufacturing. However, to further develop this technology, the maturity of the PDKs needs to be improved. This requires an orchestrated effort between foundries at one side, developing more capable and stable processes and implementing more design, process and test information in PDKs, as well as software vendors at the other side, improving the tools and flows to be able to use more information from the foundries to support design for manufacturing, yield and cost.

INTRODUCTION

The Electronic-Photonic Design Automation (EPDA) Technology Working Group (TWG) focuses on improving the design methodologies for scalable integrated electronic/photonic design. One of the overarching goals for improved methodologies and design tools, including Electronic Design Automation (EDA) and Photonic Design Automation (PDA) software, is to increase the number of electronic Integrated Circuit (IC) design teams in the world to integrate photonic functions into their systems, such as Application-Specific Integrated Circuits (ASICs) and System on Chips (SoCs), without requiring low-level physics design and need for the staff with Ph.D. degrees in Photonics. There is a need to make integrated photonics design easier by putting the low-level physics burden into the design tools and models. Another goal is to enable a robust Integrated Photonics market. This goal includes analyzing existing methodologies and defining better ways (or standards) for the various forms of design data to move between the various design "steps" of a methodology. The chair of this IPSR-I TWG is Twan Korthorst: twan @synopsys.com.

The intention of this roadmap chapter is to identify the most critical problems and to prioritize the development of solutions to help the PIC designer community to decrease the turnaround times of creating new designs for their products.

This developing designer and engineering community consists of individuals with different training backgrounds, education, and experience.

- Electronic IC Designers and Engineers
- Photonic device and process developers
- Photonic IC Designers

The electronic design community is large and has years of experience with continuously improving commercial design tools. The photonic design community is relatively small and until recently used "homegrown" design tools or tools developed for experts and researchers.

Although photonic ICs are manufactured with the same type of technologies as traditional electronic ICs and a verified mask layout is also the final step of the design flow, it is important to understand the differences between designing an electrical IC and a photonic integrated circuit or PIC. Given the nature of the underlying physics, a PIC is more like an RF-IC operating at very high frequencies. These differences drive the need for special photonic design automation (PDA) solutions in addition to existing electronic design automation (EDA) solutions.

From a simplified view the design of a (photonic) IC is a sequential multi-step approach (see Figure 1) that starts with the specification and ends with a validated and verified design in a format that can be transferred to a foundry for manufacturing. These steps are made easier for designers by means of software tools and automation steps, helping them to make schematics and layouts, and to assess the performance of the designed chip. The following figure illustrates this progression:

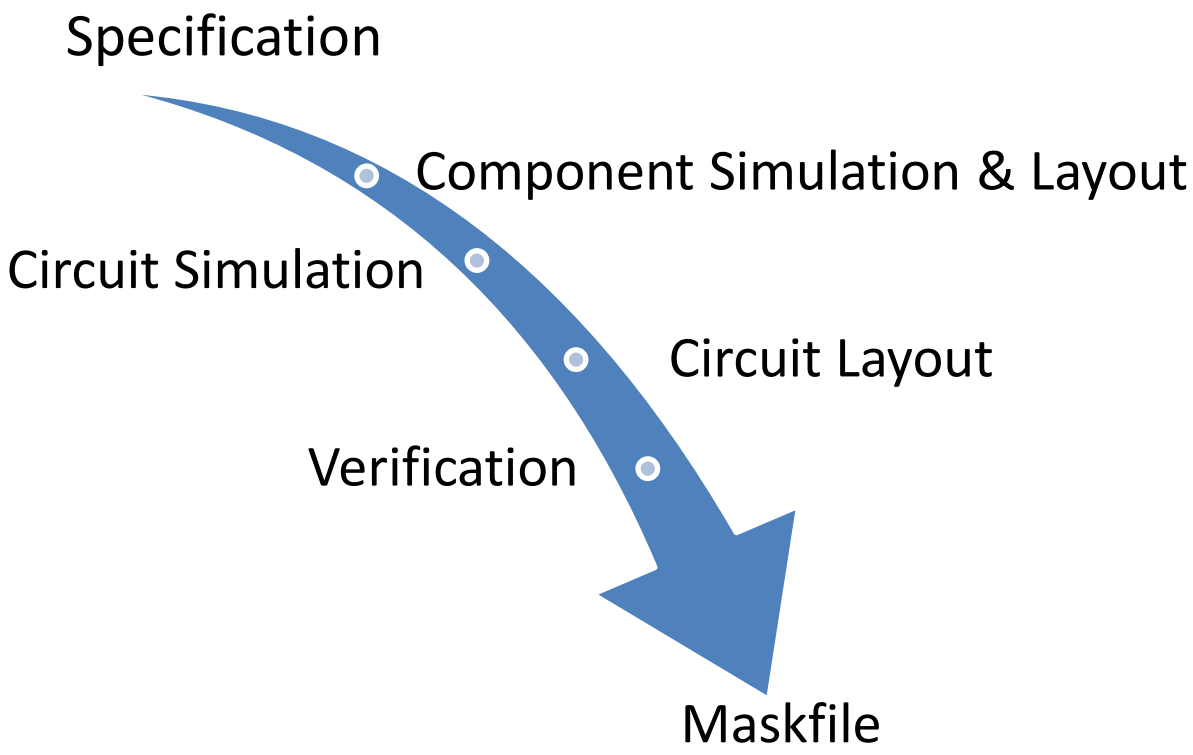

Figure 1. Overview of the steps to design a Photonic Integrated Circuit (PIC).

While the term is often used, Electronic-Photonic Design Automation (EPDA) is not yet well defined today. The term Electronic Design Automation (EDA) refers to a platform upon which the designer executes a circuit design in preparation for a foundry. Cleary, the goal should be to mimic the function of existing EDA platforms when incorporating the photonics aspect.

SITUATIONAL (INFRASTRUCTURE) ANALYSIS

Allowing designers to create a mask layout that can be submitted to a foundry is one of the key elements for the scalability of PIC technology. The introduction of Process Design Kits (PDKs) in 2008 together with the Multi Project Wafer runs has largely supported the wider application of PIC technology in domains outside the traditional telecom space and accelerated the transition from academic research into commercial manufacturing. The potential of a foundry process is, to a large extent, determined by the maturity of the technology reflected in the contents of the PDK provided to its users. Such a PDK can be compatible with design software from several vendors and contains in general:

- Technology set-up files, describing the mask layers involved in the fabrication process
- Pre-defined mask layouts and specifications for a set of Basic Building Blocks
- Mask layouts and models for a variety of more complex Composite Building Blocks
- Design and verification rules

PIC foundries that offer MPW services have a PDK containing a component library providing the mask layout for building blocks, such as splitters, modulators, detectors, lasers, amplifiers and arrayed waveguide gratings (AWG) (de-)multiplexers. In the past years, more than several hundreds of designs have been fabricated based on these PDKs. This is highly successful compared to other non-traditional semiconductor technologies. In MEMS or microfluidics, it is still very much "one process for each application." However, to further develop this technology, the maturity of the PDKs needs to be improved. This requires (1) an orchestrated effort between foundries at one side, developing more capable and stable processes and adding more information on design, process and test characteristics in PDKs, and (2) software vendors at the other side, improving the tools and flows to be able to use statistical information on process and device level from the foundries to support design for manufacturing, yield and cost.

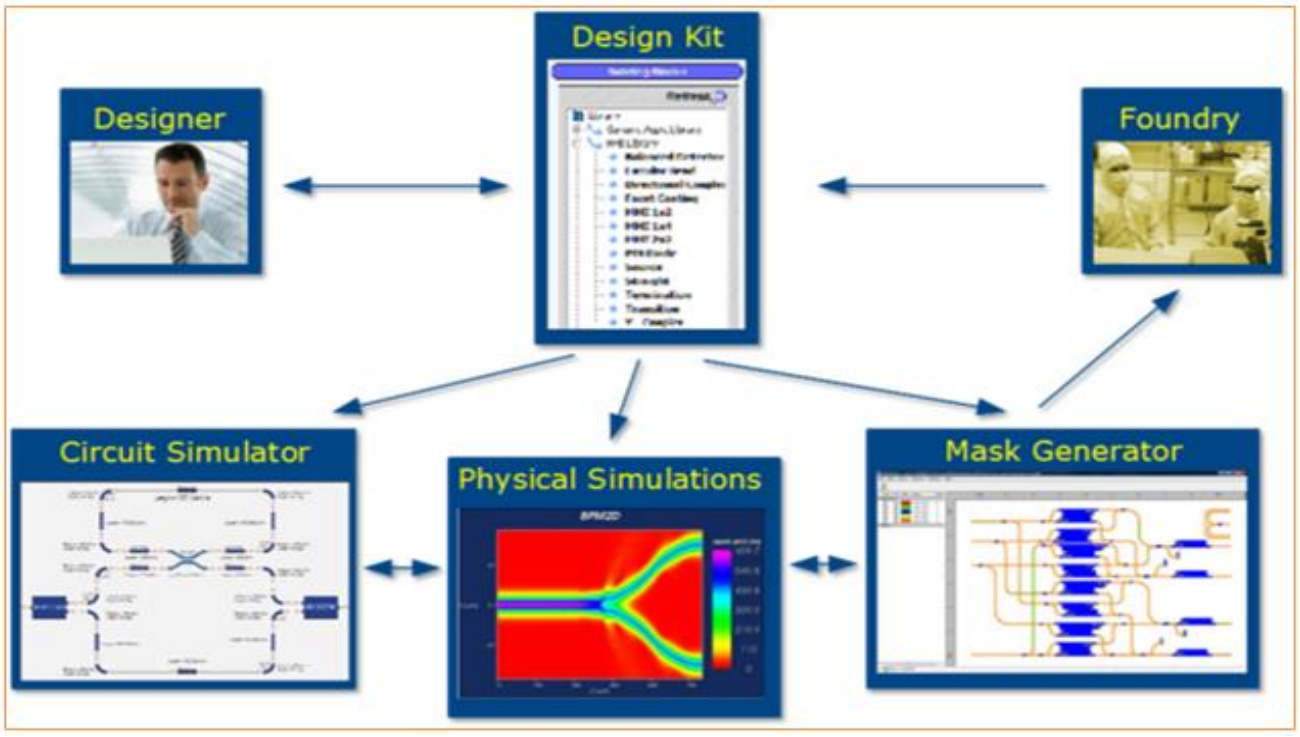

Figure 2. Simplified overview of Photonic Design Automation (PDA) functions and the central role of the PDK.

The design manual that accompanies a PDK already contains some data on component performance, however, these specifications are often not fully complete. Furthermore, the effects of statistical variations are usually missing in the specifications. To obtain reliable statistical data for the performance of building blocks, automated component characterization and component performance tracking has to become a standard procedure at the foundries and eventually at the assembly and packaging providers.

Laws of Physics

As highlighted before, photonics is not the same as electronics. Photons are not the same as electrons and the associated physics is different. Remember that the telecom C-Band that is used in optical fiber communication is using the 1550nm wavelength, corresponding to a frequency of 193THz. This requires different time steps when simulating circuits. Optical signals can be bi-directional and multi-modal, requiring other simulation techniques and solvers. Photons don't like corners, so geometries tend to be curvilinear and the layout together with physical verification tools need to be able to cope with this peculiarity. Therefore, several dedicated solutions have been developed since the early 1990s to replace home-grown tools used in academia and research departments.

Design Tools and Flow

To feed such a design sequence shown in Figure 1, foundries provide all the required technical information about the manufacturing process and available building blocks, including all the relevant specifications in the PDK. A PDK is essentially a plug-in library for a given design environment containing the required information to successfully create and validate designs based on previously verified building blocks. A PDK supports re-use of knowledge and promotes tool interoperability, while ensuring building block performance and thus circuit yield. PDKs can also be extended by adding the design libraries from external design houses and IP providers or the designer. In CMOS design, the introduction of this PDK infrastructure revolutionized the efficiency of design development and allowed a much higher design complexity. As the integrated photonics ecosystem is in its childhood compared to electronics, the maturity of the tools and PDKs is also at its early stage today.

Expertise level

It is important to keep in mind that the level of training for a future PIC designer at the EPDA level should not require a PhD in photonics or its equivalent. EDA platforms have achieved this level by providing tools that employ simplified abstracted models of circuit elements to construct complex circuits. The simulation remains at this compact model level, which is provided in a uniform way through the PDK. These models are developed outside of the EPDA design platform and typically rely on more sophisticated simulation tools and require expert users. As an example, when a new electrical device, e.g. a novel transistor structure, is required, a development team will use the tools already comprising simulations of the topology and underlying structure as well as fabrication processes. These so called TCAD tools have been used to construct compact models to be utilized in the design platform. This is not to say that these tools are not important to the development of ICs. The existence of these tools is vital and should not be restricted in any way by the confines of an EPDA environment.

Tool Maturity

On the uptake of silicon as a dominating material platform in photonic ICs, in addition to traditionally used materials like silica (also known as planar lightwave circuits or PLC), silicon nitride (SiN) and indium phosphide (InP), electrical IC designers are now entering this field. These designers are used to EDA solutions from various vendors and are trying to perform the required design steps with these tools that are not built for photonic design. This approach often requires a high-level customization and a combination of separate point solutions in an inefficient way. Additionally, there is a need to address the demand for designing the electronics and photonics parts in closer conjunction and for these reasons EDA and PDA vendors started to work together to combine the best of both worlds, to create complete, mature and trusted electronic-photonic design automation (EPDA) environments.

Circuit Simulation

Models to simulate building blocks at the circuit level for both frequency and time domains are becoming more available, thus enabling a full design flow from circuit design to layout verification. To further develop the automation of PIC design, tools and flows activities are ongoing at several software vendors, design houses and academia, supporting PDK driven layouts as well as custom designs within the boundaries of the fabrication technology. Depending on the end-application and complexity of the system-under-design (e.g. the number of components, the required optical and electrical routing, or the balance between the components of both types) the most applicable tools or flows might be different.

Component-level simulations

Component-level simulations to support PDK creation or allow designers to add their own building blocks while designing a PIC are well-developed. For passive devices that are restricted to photonic performance, there is a wide range of commercial tools that provide accurate physical simulation results. Various numerical methods can be tailored to the specific problems. However, there are fewer tools available to simulate devices that require time-domain modeling of electro-optical interactions. Proper simulation requires more in-depth knowledge about the device operation, to judge which approximations are justified.

Dedicated software exists for the simulation of integrated laser diodes based on physical parameters. Time-domain device simulations of active components, from the foundry PDK library, have become available over the last two years. Such simulations should be based on device parameters that have been extracted from the PDK library components.

Modelling of the Radio Frequency (RF) dynamic processes of electro-optical devices is very limited, and co-simulation that includes the RF electronic driver circuit as well as the component environment (package) is in its infancy.

Design Validation

Physical verification or design rule checking (DRC) needs to be implemented on two levels. Firstly, the mask layout software implements design intent check, by ensuring that parameters are within the range as specified in the design manual and that basic rules for proper circuit design are followed. Some of these are presently in place and give an early warning to designers if the rules are not obeyed. Secondly, the resulting GDSII mask files themselves are submitted for DRC to flag violations of manufacturing rules set by the foundries. Depending on the maturity of the foundry process, a smaller or larger number of such DRCs are presently in place. A much more extensive set of such DRCs should in many cases be developed, and the verification should be an automated step performed by software tools, since manual checking is labor-intensive and error-prone.

ROADMAP OF KEY ATTRIBUTE AND TECHNOLOGY NEEDS

The question is how we define the photonics part of EPDA in a practical way given its relative immaturity. To target a larger set of designers, also from the existing IC designers, the goal should be to rely mainly on compact models of an EPDA platform. While detailed modeling of photonic structures plays a more important role in comparison to its electrical analog counterpart at this point. As the photonics industry matures, this will be mostly relegated to the R&D teams and organizations rather than the design groups.

PDKs from foundries often do not have all of the required elements defined. Therefore, it is often the case that custom elements need to be created. This requires detailed modeling, which takes a considerable time to create compact models to be incorporated in the PDK as custom elements. Given this, the EPDA function, as it now exists, should not require custom platforms to accommodate detailed modeling of circuit elements, e.g. FDTD, full-wave models, etc. Instead, the industry needs to realize, at this point in its evolution, that these functions are necessary and that much more element modeling will be required until PDKs become robust enough to accommodate the vast majority of PIC designs.

In the interest of the longer-term goals, EPDA should be defined as follows:

EPDA - a suite of tools facilitating schematic capture, layout, physical and performance verification of photonic integrated circuits and systems, employing of libraries of compact models as part of a PDK.

NEAR TERM ROADMAP PRIORITIES

To address the increasing complexity of photonic circuits, design tools will have to be able to automate more designer tasks at the circuit level. In the electronic design automation space, the most common flow is called Schematic Driven Layout (SDL). The first step here is to capture the designers' intent at circuit level, perform simulation for the whole circuit and when satisfied move to the layout phase. The industry seems to be ready to move towards such a working model, but the transition has been hindered by the lack of compact models for the components in a PDK. The priority should be centered on providing the circuit capture capability, with simplified generic models, to start supporting the SDL flow, meanwhile improving the models to become more and more accurate when simulating the (full) circuit. Adding more thermal and mechanical modeling capabilities is required to design more robust circuits for a wider operating range. Another advance is to move to a full bi-directional interface between schematic and layout, to make sure that changes made at the layout level are back annotated to the intended circuit and can be reevaluated.

In addition to the improvements in the circuit design environment, more automation is required for the layout phase. When complexity goes up, more placement of components is needed and more interconnections need to be made. In electronics this is called Place and Route, and it is a significant step in the whole design process. For digital IC design it is completely automated, while for photonics the automation is at emerging stage. We expect to see more automatic layout generation from schematics, more auto-routing of waveguides (also for phase sensitive connections) and more automated DRC capabilities.

The existing commercial tools can perform this automated design rule checking, but the PDKs need to become more mature by adding additional design rules to the DRC deck to complete all the necessary checks. Finally, it should be possible to perform Layout versus Schematic (LVS) checks by taking a final mask layout design and reconstructing the intended circuit. For electronics this is a crucial step to ensure that the final design is manufacturable (after DRC) and compliant with the designers' intent. Current electronics tools are not able to perform LVS on photonics designs out of the box, due to the curvilinear nature of the designs and as the concept of "open" and "short" for electrical wires are not applicable for optical waveguides.

For most integrated design flows and extended PDKs, collaboration is a key enabler. The PDAFlow Foundation (www.pdaflow.org), created in 2013 includes many software vendors in the field as members, started to develop and maintain standards and interfaces for defining photonic PDKs that are compatible with software tools from multiple vendors and an API supporting tool interoperability. Also, the major EDA standardization organization, Si2 (www.si2.org), employed an activity dedicated to silicon photonics to address the requirements for PIC design in OpenAccess, the most widely used EDA design database and API. More recent initiatives at IEEE and by openEPDA (www.openeda.org) are illustrating the transitioning in this field and the tendency to work together to improve the design environment. Besides these achievements, bilateral collaborations between software vendors exist to develop electronic-photonic design environments and/or interface layout and simulation tools. Further automation of the design flow will require more enhanced simulation routines combining time-domain, frequency domain, co-simulation of electronic and photonic components, and consideration of parasitic effects, such as crosstalk and scattering. However, the focus needs to be on adding simulation capabilities to incorporate process and performance variations throughout the whole design flow. This requires fabs to add this information into their PDKs and the software tools to be able to use this information to perform full yield analysis.

Based on the WTMF and IPSR-I working group meetings the following priorities have been identified:

The PIC designer community need the following in addition to what is available today:

1. Information from the fabrication processes
    a. Including process variations
2. An automated (and dynamic) interface between electronic and photonic design tools
3. Improved verification capabilities
    a. Consistent design rule checking (Need: shared language for DRC rules)
    b. Post layout (circuit) simulation
    c. Layout versus Schematic validation
4. Interfaces between device and circuit simulation tools
    a. Not “copy-paste” from one tool to another
5. Ability to extract and/or deal with “parasitics”
    a. Reflections, scattering/straylight, cross-talk, RF, thermal

The PDK developer community need in addition to what is available today:

1. Interface with test frameworks
    a. Standards for measurement information exchange to build compact models from the same data sets to different software tools.
    b. Interfaces between layout tools and test automation tools.

Finally, there is an emerging activity to develop and provide design IP for PICs. Making third party libraries available by means of an agreement upon framework will support the acceleration of re-use of IP and shorten PIC development cycles.

Prioritized development milestones (<2025)	Relative Priority
1. Interfaces / integration between electronics and photonic design tools	
a. To enable non-expert designers	Critical
b. To allow co-design of electronics and photonics	Regular
c. To enable E/O co-simulation and co-optimization	Desirable

Prioritized development milestones (<2025)	Relative Priority
2. Improved verification capabilities	
a. Consistent Design Rule Checking (DRC)	Critical
b. Post Layout Simulation	Critical
c. Layout versus Schematic (LVS)	Critical
3. Automated interfaces between device and circuit simulation tools, to allow custom design	Regular
4. Ability to exctract and/or deal with 'parasitics'	
a. Optical: reflections, scattering, straylight, cross-talk, noise	Desirable
b. Electrical: RF up to 100GHz	Regular
c. Thermal: circuit level, device level, cross-talk	Regular

Short Term Solution Directions for identified Critical Needs

Simplify Design by focusing at the Circuit level

- Introduce Schematic Driven Layout
- Automate Layout (Place & Route, Synthesis)
- Back annotation of actual layout implementation for post layout simulation
- Improve PDKs

Improve Design by enhancing DRC and LVS

- Remove false errors in DRC
  - Support for curvilinear features
  - Addressing grid snapping
- Develop photonic LVS capabilities
  - A short is not a short
  - Waveguides close to each other can be a short
  - Photonic device recognition and parameter extraction

LONGER TERM ROADMAP PRIORITIES

In addition, the need for design, test and packaging is becoming more prominent. This includes, for instance, the ability to simulate (RF) signals to and from the chip throughout the package to a printed circuit board or an electrical die in the same package. But also, optical (ray tracing), mechanical, electrical (charge mobility) and thermal modeling of a complete sub-system or system are required to develop more complex and complete systems making use of PICs.

There are several subjects which are of essential importance and can be qualified as the critical challenges for the next 5 – 10 years.

1. Design flows and tools must be developed for all levels and interchangeable between the several photonic technologies like InP, SiN, SOI, GaAs, PLC and Polymers.

2. The merge of semiconductor electronics with photonics becomes of extreme importance. All photonic technologies and the tooling must be useable for photonic-electronic co-design.
3. The intermediate coherence between all of the device aspects, like thermal management, performance of the PICs and ICs, packaging and co-designs of electronics, becomes very important.
4. The predictability and reproducibility must be improved for all technologies and levels to be able to deliver to mass markets with the mature expectations for product quality and reliability.
5. And finally, but not last, enough educated designers that are able to design PICs and PIC-based systems using the developed EPDA solutions.

Technology Development Needs (~2030)

Scale the design environment to support System Design

- Software Tools to address the design of die/chiplet/interposer configurations
- Software Tools to address packaging and assembly of modules
- PDKs or Assembly Design Kits (ADK) to be completed with 'models' capturing electrical, mechanical, optical, thermal phenomena and performance
- Tools should allow for broadly understood design for product (DfX) accounting for Design for Test, Design for Package, Design for Manufacture

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