INP AND III-V COMPOUNDS

Contents

EXECUTIVE SUMMARY

III-V semiconductor compounds form the core material systems of a wide range of discrete and eventually fully integrated photonic components (lasers & optical amplifiers, modulators, photodetectors, and passive-optical functions) and also high-performance electronic devices. A key feature of III-V compounds is that they exhibit a direct bandgap enabling efficient generation and amplification of light, as opposed to indirect bandgap semiconductors like silicon and germanium. Since the sixties of the previous century this has resulted in the development of a wide range of semiconductor laser types (CW, tunable, multi-wavelength, pulse, frequency-comb, single photon) for use as transmitters. Tuning the electronic band gap of the material by alloying different III-V compounds, enables the adjustment of the wavelength of the light to the required value within a fairly broad spectral NIR range. Materials based on GaAs (~ 850-1100 nm) and InP (~ 1200-1700 nm) are the most prominent systems in use, largely driven by fiber-optic communications. Thanks to this application field InP has achieved a superior role in integration of semiconductor lasers with a variety of structures enabling manipulation of the photons in photonic integrated circuits for a wide range of functionalities.

InP-based PICs have become firmly established in the marketplace, with suppliers and users shipping or deploying large numbers of complex PIC-enabled products today. A major advantage of InP-based PICs is their ability to integrate arrays of lasers and optical amplifiers in a single chip. Furthermore, integrated InP based modulators have demonstrated superior performance (driving voltage, efficiency). GaAs is mainly applied in VCSELs and VCSEL arrays. The present roadmap is restricted to InP technology, in future versions we intend to include more information on other III-V materials as well.

CURRENT STATUS

InP-PIC enabled transceivers already account for >1B€ market share. A major portion of this market is served by vertically integrated companies, but generic foundries have been established which have the potential to broaden the application of PICs to module and systems manufacturers who cannot afford the large investments for a cleanroom fab and development of a qualified proprietary manufacturing process.

MAIN CHALLENGES

A challenge for InP is the lack of a large-scale manufacturing infrastructure. Although the existing infrastructure is adequate for today's market, the expected increase in growth will require major investments in scaling the infrastructure for manufacturing and testing to align with the expected market size. Scaling laws and scaling costs for InP monolithic integration are similar to those of silicon fabs. With the growing demand for high performance PICs with a high degree of integrated functionality and flexibility, it will be feasible to allocate the required investments to scale to high-volume manufacturing and hence reduce the costs for InP PICs.

As highest technical priority we see the adaption of today's manufacturing equipment, most of which is still operated manually, to fully automated operation. For increased operational efficiency and performance, it is important to move to larger wafer sizes: 4", which is already in use today, and 6". In the longer term, transfer from InP-substrates to silicon substrates is envisaged, while keeping the photonic layer in InP and its compounds. This will enable transitioning the processing of InP PICs to 8" and larger wafers but will demand processing equipment with new capabilities. Improved manufacturing capability in terms of precision and resolution will ultimately enlarge the component design space and advance building block performance.

Another priority is in PDK-development and automated testing. First PDK's (Process Design Kits), which offer designers a variety of building blocks without the need for a deep knowledge of semiconductor technology, were introduced for InP-technology more than a decade ago, but still require further development: more and more accurate building blocks and better simulation capabilities. PDK development and automated testing for InP has a large synergy with silicon photonics.

The future needs with respect to the basic technology to allow for improved performance highly depends on the photonic building block under consideration. The ultimate performance achieved by each building block will be largely determined by the integration platform capability in close consideration to application specific requirements and the trade-offs of complexity and performance costs, manufacturability and yield.

NEEDS:

Needs < 5 years
- Fully automated process equipment (lithography, epitaxy/deposition, etching) with cassette loading
- Improved reproducibility of epitaxy/deposition and etching (<1%)
- Reduced defect density in epitaxial (re)growth
- 193 nm lithography tools for 4" wafers
- Lithography resist selectivity
- Improved passivation technology for non-hermetic packaging
- Test standardization and automation at building block and circuit level

Needs 5-10 years
- Move to larger wafers (6")
- Higher integration densities using membrane technologies

Needs > 10 years
- Move to InP processing on silicon substrates (8" and larger)

INTRODUCTION

InP-based PICs have become firmly established in the marketplace, with suppliers including Lumentum, II-VI/Finisar, Infinera and Sumitomo deploying large numbers of complex PIC-enabled products today. InP-PIC enabled transceivers already accounted for a 1B€ market share in 2015 according to market research by LightCounting and the technology is predicted to account for 35% transceiver market share by value (5% by volume) in 2021. The breakthrough has been made with the roll-out of 100 Gb/s per wavelength link, and the indications are that the InP-PIC market share will continue to increase substantially in applications where device performance is critical.

Discrete devices are produced at volumes in the order of 10M per month on 3" and 4" wafers. Low complexity PICs, comprising of monolithically integrated lasers and modulators, are ramping up volume. The current equipment infrastructure is adequate for the cost-performance levels demanded by today's optical communication's market, but the volumes and costs required by emerging applications, especially inter and intra data center interconnects, will put increased pressure on manufacturing equipment and process performance. Furthermore, the requirement to reduce ramp-up time from first design to production calls for increased up-time in production process and predictability.

An important development in this respect is the emergence of "generic" platform technologies, which support development and fabrication of high-performance PICs for a wide range of applications in highly standardized integration processes. The generic approach leads to technology de-risk, a large reduction in the costs of prototyping since it enables sharing the costs of PIC fabrication among many users, and by offering access to a qualified fabrication process which supports volume production. This leads to a substantial lowering of the entry costs for new applicants in the field and opening PICs to new applications and market sectors. Generic open-access foundry service has been pioneered in Europe for InP and silicon photonics since 2007 and is presently experiencing a rapidly increasing interest worldwide. Open access to MPW PIC runs in foundry processes is now offered by a few commercial foundries and several national research centers.

The foundry approach with well-developed processes will have performances that are on par or close to those of highly-customized processes. For specific applications, optimization and customization might be required to allow tuning the offering to achieve ultimate performance. When production volumes are sufficiently large, users of open access foundry processes may decide to customize their foundry process to reach a specific PIC performance improvement. However, by choosing to start product development and validation through a foundry process, the investments in development and qualification will be lower compared to starting from scratch and will occur at a later stage when the risk in the expected market size is reduced.

The most commonly acknowledged market sectors addressable by PIC technologies are optical transceivers, fiber optic sensors, OCT, BioMEMS and LIDAR. The front-runner market is transceiver technology, which currently receives considerable attention due to a pressing need from internet traffic growth and accelerated data center deployments. Fiber-optic sensing offers a considerable growth opportunity with drivers from the oil industry as well as structural engineering, industrial metrology and aerospace. Compound annual growth rates (CAGR) of order 10% to 20% are observed for photonic solutions in such markets. Medical segments, such as optical coherence tomography (OCT) through to BioMEMs technology, also see considerable growth.

The increased need for free-space mapping and ranging is driving down the costs of solid-state LiDAR technologies, with likely impact in autonomous driving, robotics, vision and virtual reality systems. Although there are commercial implementations already available today, prices are still too high for adoption into large-scale applications. Eye-safety requirements and their potential for advanced beamforming and signal processing make InP-based PICs an important technology for use in LIDAR systems. As the InP-PIC technology deploys across multiple markets and volumes increase, the corresponding price reduction should enable the use of PIC technologies in larger, more cost-sensitive markets.

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS

In this section we describe the present status of the most important building blocks in InP-PICs and the expected evolution of the requirements in 5, 10 and 15 years. The tables are given for PICs operating in the C-band. We consider the addition of similar information for other wavelength bands, such as the O- band and L-band, important but data are not yet available for this edition of the roadmap.

The most important basic building blocks are waveguides, optical amplifiers, electro-refraction and electro-absorption modulators, and detectors.

For the **waveguides,** key properties are propagation loss and minimal bending radius, wavelength and polarization dispersion, which should be very low for polarization independent operation of components based on those waveguides.

For **optical amplifiers**, basic building blocks in any laser, the important parameters are gain and gain bandwidth, output power and efficiency (which is closely related to the transparency current), maximum operating temperature, and polarization properties. The latter may be of less importance in lasers, which are usually TE polarized.

The most important **modulator** types are electro-refraction (phase) and electro-absorption (amplitude) modulators.

Electro-refraction modulators are often applied in a Mach-Zehnder configuration. Important properties are electro-optic efficiency, optical loss, linearity and modulation bandwidth. Good modulators have low insertion loss (<1 dB) and high bandwidth (with a traveling wave electrode > 30 GHz). The modulation voltage is dependent on the length: for low voltages (few Volt) the length is in the order of 1 mm. InP modulators show superior performance in comparison to other technologies.

Electro-absorption modulators are significantly smaller than Mach-Zehnder modulators (size of order 50-100 µm). Due to their small size they can have bandwidths > 50 GHz, but as they operate close to the absorption edge of the semiconductor, they have significantly higher losses than Mach-Zehnder modulators, lower spectral bandwidth, and higher chirp[1] (though zero chirp is possible at certain operating conditions), which makes their commercial deployment in links > 80 km less suitable for high-speed communication in the C and L band.

Detectors show responsivities close to 1 A/W in the C-band, in combination with bandwidths > 40 GHz, and dark currents in the order of 1 nA.

The most important **composite building blocks** are lasers and passive components like MMI-couplers and AWGs. Most platforms support a variety of **lasers**: single-frequency, continuous wave (CW) and short-pulse lasers, tunable and multi-wavelength lasers. Output powers of a few tens of mW are available in most platforms. Laser linewidths are strongly dependent on the laser configuration, ranging from a few MHz to <100 kHz for sophisticated designs. Many laser designs have been reported covering the whole C-band. Energy (wall-plug) efficiencies range to 20% for higher output powers, for low output powers efficiencies are lower. With high-resolution lithography, insertion losses of **MMI couplers and AWGs** can be well below 1 dB (for the central AWG channel).

The tables below address the state-of-the art and future needs for each building block to meet a wide range of applications. The performance metrics are based on current understanding of fundamentally achievable performance of InP building blocks without consideration of a specific application. The ultimate performance achieved by each building block will be largely determined by the integration platform capability in close consideration to application specific requirements and the trade-offs of complexity and performance cost, manufacturability and yield.

[1] *Chirp is unwanted phase/frequency modulation induced by an intended amplitude modulation*

Basic Building Blocks					
Component property	**2020**	**2025**	**2030**	**2035**	**2040**
1. Waveguide					
Propagation loss / PDL [dB/cm]	1-1.5	0.5-1.0	0.3-0.5	0.3-0.5	0.3-0.5
Minimum bend radius [μm]	100	50	25	10	10
Bend loss per 90 degree [dB]	0.5	0.2	0.1	0.01	0.01* *Transition to high-contrast WG platform
Wavelength dispersion [(Δn/n)/nm]	1.7×10^{-4}	1×10^{-4}	0.5×10^{-4}	$<0.5 \times 10^{-4}$	$<0.5 \times 10^{-4}$
Waveguide transparency (<1.5 dB/cm loss) / wavelength range [nm]	1200-1640	1200-1640	1200-1640	1200-1640	1200-1640
Mode diameter [μm, FWHM]	1.5x1.0	1.5x1.0	1.5x1.0	0.5 x 0.5*	0.5 x 0.5* *Transition to high contrast WG platform
Back scattering [dB/mm]	-40	-40	<-50	<-50	< -50
2. SOA					
SOA Gain [dB]	15	20	25	25	> 25
Polarization Dependent gain (PDG) [dB]	3	2	1	0.5	< 0.5
Gain bandwidth [nm]	35	50	100	150	> 150
Maximum gain ripple [dB]	2	1	0.5	0.1	0.1
3-dB gain saturation output power [dBm]	10	13	16	16	16
Maximum current density [kA/cm^2]	10	12	15	15	15
Operating temperature range [°C] Operation not at max. gain, within 10 dB drop	20…45	10…70	-40…85	-40…85	-40…90 p
Noise figure [dB]	8	6	4	4	4
3. Electro-refraction modulator					
Electro-optic efficiency [V mm]	4	2	1	<1	< 1
Insertion loss [dB]	3	3	1	1	< 1
RF 3-dB Bandwidth [GHz]	50	70	100	>100	> 100
Optical 3-dB Bandwidth [nm]	40	50	70	100	> 100
Spurious free dynamic range of second harmonic distortion SFDR (SHD) [dB x $Hz^{1/2}$]	50	80	90	>100	> 100
Max length [μm]	3000	2000	1000	1000	1000
Impedance [Ω]	25-50	25-100	25-100	25-100	25-100
4. Electro-absorption modulator					
Minimum insertion loss [dB]	3	1	1	1	< 1
Minimum Extinction ratio [dB]	12	20	20	20	> 25

RF 3-dB Bandwidth [GHz]	35	50	70	100	> 100
Optical 3-dB Bandwidth [nm]	10	15	15	15	15
Max length [μm]	150	100	100	100	100
Small Signal Chirp [unity]	2	1	0	0	0
5. Thermo-optic phase modulator					
Power for π phase shift [mW]	90	50	20	20	< 20
Insertion loss [dB]	1	0.5	0.1	0.1	0.1
Extinction ratio [dB]	20	25	25	25	> 25
Response time [μs]	100	50	5	5	> 5
6. Photo detector					
Responsivity [A/W]	>0.8	>0.9	>0.9	>1	> 1
Bandwidth (electro-optical) [GHz]	40	70	100	>100	> 100
Dark current [nA]	1	1	1	1	< 1
3-dB Saturation power [mW]	10	20	20	20	> 20
Polarisation dependence [dB]	<1	<1	<1	<1	< 1
7. Tunable Bragg reflector					
Coupling coefficient [cm^{-1}]	100	200	200	200	200
Absolute wavelength control (GHz) during tuning of grating	5	1	0.5	0.5	0.5
Coupling coefficient precision [/cm]	±10	±5	±1	±1	±1
Apodization feature size [nm], Sub-lambda	200	100	20	20	20
8. Grating couplers					
Insertion Loss [dB]	3	2	0.5	< 0.5*	<0.5* *Membrane
1-dB bandwidth [nm]	30	30	30	30	30
Parasitic back reflection [dB]	-15	-20	-40	-40	-40
9. Polarization rotation section					
Insertion loss [dB]	1	0.5	0.5	0.5	<0.5
Optical bandwidth [nm]	30	50	100	100	100
Physical length for 90° rotation [μm]	1000	500	100	100	100
Polarization extinction ratio [dB]	10	25	30	40	40
10. Spot size converter					
Input/Output mode diameter [μm]	10	10	10	10	10
Insertion loss [dB]	2	1	0.5	0.1	< 0.1
Polarization dependent loss [dB]	1	1	0.5	0.5	< 0.5
Physical length [μm]	1200	400	200	100	< 100
Parasitic reflectivity [dB]	<25	<30	<30	<30	< 30

Composite Building Blocks (CBBs)					
1. (Tunable) CW laser					
Output power [mW]	50	50-70	70-100	>100	> 500
Tuning range [nm]	40	40-50	100	150	150
Tuning speed [ms/µs/ns]	µs	µs	ns	ns	ns
Linewidth [kHz]	200	100	10	1	< 1
Relative intensity noise [dB/Hz]	-145	-150	-155	-160	< -160
SMSR [dB]	>40	>50	>50	>50	> 55
Operation temperature [°C]	25	45	70	>85	> 90
3. MMI couplers					
Excess Loss [dB]	0.5	0.3	0.2	0.2	< 0.2
Splitting ratio accuracy [dB]	0.3	0.2	0.1	0.1	< 0.1
Spurious reflectivity [dB]	<-30	<-40	<-40	<-40	<-40
Optical bandwidth [nm]	40	60	80	100	>100
4. MMI reflectors					
Insertion loss [dB]	1	0.5	0.3	0.2	< 0.2
Reflection/transmission ratio accuracy [%]	10	5	3	1	> 1
Optical bandwidth [nm]	40	60	80	100	100
5. AWG (de)multiplexers					
Excess loss [dB]	5	3	2	1	< 1
Maximum number of channels	10	20	30	40	> 40
Minimum channel spacing [GHz]	200	100	50	50	> 50
Excess loss for outer channels [dB]	3	2	1	0.5	0.5
Crosstalk [dB]	-25	-30	-35	-40	< -40
8. Polarisation splitter/coupler					
Insertion Loss [dB]	1	1	0.5	< 0.5	< 0.5
Rejection unwanted polarisation [dB]	10	>20	30	> 30	> 30
9. RF interconnection					
3 dB frequency at 2 mm length [GHz]	50	70	80	>100	> 100
Propagation loss at maximum frequency [dB/mm]	0.3	0.3	0.3	0.3	< 0.3
10. Mach-Zehnder modulator					
Electro-optic efficiency [V mm]	4	2	1	<1	< 1
Insertion loss [dB]	8	5	3	1	< 1
RF 3-dB Bandwidth [GHz]	50	70	100	>100	> 100
Electrical return loss [dB]	<-10	<-10	<-15	<-20	< -25

CRITICAL (INFRASTRUCTURE) ISSUES

For manufacturing equipment special attention is required in the following fields:

WAFER HANDLING

Due to the fragile nature of InP, robotic wafer handling is required throughout the production line to reduce instances of breaking and accumulation of particles. To meet yield expectations in high performance PICs, InP PIC production equipment should support cassette-to-cassette loading.

LAYER THICKNESS AND ETCH DEPTH CONTROL AND UNIFORMITY

Optical waveguide properties are very sensitive to waveguide dimensions, requiring well defined process windows delivering dimensional control down to the few nm level. As an example, a 1-nm variation in the width or height of high-contrast waveguides leads to 100 GHz wavelength shift in wavelength selective devices, which means that nm-scale variations in waveguide dimensions over the wafer can have a significant effect on the component properties. Enhanced in-situ measurement capabilities are needed to control the layer growth in epitaxy and PECVD and the etch depth in the etching tools. This will enable systematic process control and optimization across wafer topologies. In-line particle detection capabilities are expected to accelerate process control to improve fabrication yields.

TOOL-STATUS CONTROL

Accurate production tool status control and compensation, including self-cleaning methods are important for increased throughput and process uniformity. Self-cleaning will be required for epitaxial equipment, and increased reproducibility in terms of layer thickness and materials composition with control down to ± 1% in the coming years and an order of magnitude better on the longer term (see tables on technology needs).

LITHOGRAPHY

It is important that the resolution and reproducibility of 193 nm DUV lithography becomes available also for wafer diameters below 200 mm, including 4” and 6”. Because of its small depth of focus, high resolution optical lithography has increased requirements on wafer flatness, and there is an insufficient number of suppliers meeting the specifications for precision lithography.

TESTING

Testing of process parameters (geometrical, optical and electrical) should become available as early in the fabrication as possible. Automatic testing of dedicated test structures should be performed at wafer level. New inspection methods and analytics are needed to correlate in-line test, off-line product test and product release test in a generic, application independent way.

PACKAGING AND ASSEMBLY

Efficient and compact Spot-Size converter arrays and etched angled facets are important for low-loss low-reflection coupling to fibre arrays and multi-port interposers. For ease of coupling and assembly the angled facets should be positioned such that the output beams leave the chip normal to the chip edge. For efficient coupling to rf-electronics, rf-waveguides should be integrated in the PIC design.

TECHNOLOGY NEEDS

By improving on manufacturing accuracy, fidelity and reducing attainable feature sizes and tolerances, more sophisticated and more precise designs can be made on component level, leading to steady advancements of the performance metrics. Accurate epitaxy and precision lithography can lead to more capable functional actives and lower losses for passive components. Higher resolution and smaller feature sizes translate to compact components that are more energy efficient and operate at higher speeds. In this section we describe the requirements on the manufacturing technology that are necessary to realize the component performance targets listed in the section 'Roadmap of Quantified Key Attribute Needs' in a cost-effective high-volume process.

SUBSTRATES

Today, good quality 3" and 4" InP-substrates are commercially available from several manufacturers. Wafer flatness is sufficient for stepper lithography requirements. However, for high-resolution DUV lithography wafer flatness must be improved. To allow for accurate cleaving of the final chips, the output waveguides should be aligned to a crystal plane. For this, the wafer flat has to be oriented along the crystal plane which can be offered by most substrate manufacturers.

INCREASE OF PRODUCTION CAPACITY

For the expected growth of the PIC market it will be necessary to increase the wafer capacity of existing and new fabs. This can be done by increasing the size of the wafers or by further automation of the process using robots for loading and unloading machines, or by a combination of both. Semi-insulating InP-wafers of 6" are presently available, albeit with slightly larger Etch-Pit Density (EPD). However, with increased demand the quality of 6" wafers will be improved to match the quality of today's smaller wafers. The thickness of InP wafers increased in 2" wafers to 3" wafers by 340 µm to 625 µm. 4" wafers have the same thickness as 3" wafers. What happens with 6" wafers is still open.

An alternative way to reach higher wafer capacity is a fully automated fab working with 4" wafers. It is not yet clear which way is the most cost effective. A further increase to 8" wafer diameter will require a different approach in order to avoid extremely thick substrates. Here technologies for bonding InP membranes or more complex layer stacks on silicon offer an alternative route. It would still require smaller InP wafers for growing the epitaxial layer stack, but the subsequent processing could then be done on 8" or even larger wafers. The wafer bonding technique is mastered at R&D level and efforts are made to make this technology more broadly available.

InP Substrates	[unit]	2025	2030	2035	2040
Wafer diameter	mm	150	150	200[2*]	> 200 [2] *Epi reactor development necessary
Total Thickness Variation	µm	1	0.5	0.5	< 0. 5
Etch Pit Density of SI InP:Fe	cm^{-2}	$< 5.10^3$	$< 1.10^3$	$< 1.10^3$	$< 1.10^3$
Minimum resistivity SI	Ωcm	$>10^7$	$>10^7$	$>10^7$	$> 10^7$
Flat orientation	degrees	±0.01	±0.01	±0.01	±0.01

[2] 200 mm wafers assume that the InP wafer stack is bonded on a silicon substrate

EPITAXY

For commercial epitaxy reactors layer thickness and composition reproducibility are in the order of a few percent. In the coming decade this should be improved by an order of magnitude to improve the yields for highly demanding components. Further, it is important to reduce the number of defects, especially in regrowth steps.

This will require in-situ cleaning procedures both for the reactor chamber and for the wafer surface in combination with in-situ monitoring of particles and their distribution on the wafer. For improving operational reproducibility, automatic loading and unloading of reactors is of key importance. Parallel to the increase in performance, operational techniques will have to be developed for measuring any improved performance and optimize processes and methods.

(Epitaxial) growth/layer deposition	**[unit]**	**2025**	**2030**	**2035**	**Comments**
Layer thickness uniformity	%	± 1	± 0.2	± 0.1	Over the whole wafer, with edge exclusion tbd, assuming wafer size below, large scale reactor
Layer thickness reproducibility	%	± 1	± 0.2	± 0.1	From run to run
Layer composition uniformity	PL (nm)	± 1 nm	± 0.5	± 0.1	With wafer exclusion at wafer edge
Layer composition reproducibility	PL (nm)	± 1 nm	± 0.5	± 0.2	From run to run
Doping concentration uniformity	%	± 10	± 5	± 1	Over the whole wafer, exclusion edge
Doping concentration reproducibility	%	± 5	± 5	± 1	From run to run
Other dopant materials	name	C, Be, Mg	C, Be, Mg	C, Be, Mg	Alternate stable/abrupt p-dopant precursor
Defect/particle density	cm^{-2}	5	2	1	Depends on particle size < 1-20 microns; for one growth run
Wafer diameter	mm	150	150	200	

DEPOSITION AND ETCHING

The most important properties of deposition and etch equipment are the reproducibility and uniformity of layer thickness and etch depth. Waveguide properties like propagation constant and polarization dispersion are extremely sensitive to width and thickness variations, down to the nm-level. In order to approach that, reproducibility and uniformity will have to be improved by an order of magnitude in the coming decade, from a few percent today to one or a few tenths of a percent in ten years. In situ monitoring of layer thickness, etch depth and tool status will be necessary to achieve such performance. Just like for epitaxy reactors, automatic (robot) loading and unloading is crucial for reproducible operation.

Dry etching	**[unit]**	**2025**	**2030**	**2035**	**Comments**
Side wall roughness (rms)	nm	5	2	1	< 2 microns
Side wall angle accuracy	degree	± 1	± 0.5	± 0.2	
Etch depth uniformity	%	± 1	± 0.5	± 0.1	Over the whole wafer with edge exclusion
Etch depth reproducibility	%	± 1	± 0.5	± 0.1	From run to run
Maximum etch rate	μm/min	5	10	10	Chemistry dependent
CD* Loss	nm	10	3	1	
CD* uniformity	nm	5	3	1	Over the whole wafer with edge exclusion
CD* reproducibility	nm	10	3	1	From run to run
Smallest slot width	nm	100	50	20	Over the whole wafer; will be aspect ratio dependent
Smallest line width	nm	100	50	20	Over the whole wafer; may differ for dense and isolated lines
Minimum grating pitch	nm	200	180	180	Over the whole wafer

*) Critical Dimension

Deposition of dielectrics	**[unit]**	**2025**	**2030**	**2035**	**Comments**
Layer thickness uniformity	%	± 1	± 0.5	± 0.2	Over the whole wafer
Layer thickness reproducibility	%	± 1	± 0.5	± 0.2	From run to run

Metal deposition	**[unit]**	**2025**	**2030**	**2035**	**Comments**
Temperature budget	[K]	<350	<350	<350	Compatible with lift-off patterning
Layer thickness Uniformity	%	2	1	1	
Layer thickness reproducibility	%	± 2	± 1	± 1	From run to run

LITHOGRAPHY

For good lithography performance and to avoid damage during exposure, it is important to remove contact lithography from the process flow and replace it by projection lithography. Today resolutions up to 250 nm can be achieved with stepper lithography. For non-flat surfaces (e.g. after several epitaxial overgrowth steps) and higher resolutions, e.g. in gratings, E-beam lithography is used. Because this is a direct-write technology, it is difficult to scale it to very high throughput without installing a large number of machines. Consequently, optical lithography

is a better option provided that processing allows for a sufficiently flat surface morphology. For the realization of the resolution required for gratings, 193 nm DUV lithography provides an important solution. This resolution is available in scanner lithography machines. However, today these machines cannot handle wafers smaller than 6". ASML has adapted one machine for handling 3" and 4" which is presently installed at the Nanolab cleanroom at TU Eindhoven. On this machine high quality gratings and low-loss AWGs with very narrow (100 nm) inter-waveguide gaps have been demonstrated. An additional advantage of DUV scanners is the process control and reproducibility, which is significantly better than for E-beam lithography. However, these machines are not yet commercially available. For high-performance high-volume manufacturing of PICs it is of utmost importance that such technologies become available in InP PIC process lines.

Stepper/scanner Lithography	**[unit]**	**2025 years**	**2030**	**2035**	**Comments**
Overlay accuracy	nm	20	10	5	
Resolution	nm	100	50	20	Needs technology development
Required Wafer Flatness	μm ttv[3]	1	1	1	
Required Wafer Flatness	μm ttv	0.5	0.2	0.2	
CD Loss	nm	10	3	1	
CD uniformity	nm	10	3	1	
CD reproducibility	nm	10	3	1	
Resist thickness	nm	100	100	100	
Smallest slot width	nm	100	50	20	
Minimum grating pitch	nm	200	180	180	

E-Beam Lithography	**[unit]**	**2025**	**2030**	**2035**	**Comments**
Overlay accuracy	nm	10	5	2	
Speed	wafers/hr	2	5	10	One response requiring 200/hr
Resolution	nm	10	10	5	
Required Flatness requirements	μm	5	5	5	
CD Loss	nm	10	3	1	
CD uniformity	nm	10	3	1	
CD reproducibility	nm	10	3	1	
Smallest slot width	nm	100	50	20	
Minimum grating pitch	nm	200	180	180	

OTHER PROCESSING STEPS

The impact of and interaction between annealing, planarization, passivation and other steps during wafer fabrication must be carefully considered to achieve high performance, high stability and high yield devices/PICs. Thermal annealing processes usually occur after dielectric deposition steps (e.g. to adjust film stress, hydrogen content), metal deposition (to promote adhesion and contact formation to semiconductor layers), and in some planarization and reflow processes. The optimum thermal budget (temperature and time) for each step will depend on the materials and fabrication sequence, but some values are indicated in the table below. Contact resistance is routinely

[3] ttv: total thickness variation

measured using standard PCMs but the effect of annealing dielectric and metal film stacks on other device properties can be more difficult to measure. Several steps including annealing (Ohmic contacts, dielectric and implant activation) will need to be automated to batch processes to reduce cycle time.

Exposed III-V surfaces are well-known to have poor stability of their chemical, electronic and optical properties, unlike silicon where the fabrication of extremely high-quality stable oxide – Si interfaces are reproducibly obtained. For example, exposed junctions during fabrication of lasers, modulators, detectors and other waveguides (by etching, diffusion or cleaving) will require a passivation coating which needs to remain stable (low leakage) through all remaining (thermal) steps in fabrication, packaging and reliability tests, and eventually at all operating conditions. The pre-cleaning and deposition of the passivation layer should not degrade the target surface roughness or optical loss of etched waveguides.

Integration of the basic building blocks into functioning PICs involves tapered etching or etching and regrowth as part of waveguide formation. In addition to sidewall passivation, the reflections from interfaces between different parts of the PIC waveguide need to be controlled to achieve the required insertion loss and extinction ratio in modulators, for example. Optical Time Domain Reflectometer (OTDR) measurements on singulated devices or bars are used to assess the contributions from these interfaces, but some form of on-wafer assessment using etched facets or surface grating couplers may provide a useful PCM for manufacturing control.

Annealing	**[unit]**	**2025**	**2030**	**2035**	**Comments**
Ohmic Contact formation (RTA)	[K/s]	650-700/ 20 - 200	TBD	TBD	Materials and device dependent
Dielectrics (PECVD)	[K]	725	TBD	TBD	Post deposition adjustment of H content and stress
Wafer level burn-in/screening	[K]	~450	TBD	TBD	Develop methods for PICs
Planarization	**[unit]**	**2025**	**2030**	**2035**	**Comments**
BCB (cure)	[K,hour]	500/10	TBD	TBD	Coat & cure processes adjusted for topography
Required flatness	nm	500	200	100	Will depend on etched topography across the wafer.and planarizing materials used Impacts litho CD control/uniformity

Passivation	[unit]	2025	2030	2035	Comments
Junctions and facets (PECVD)	[K]	575	TBD	TBD	Low damage conformal processes. Atomic Layer Deposition (ALD) may become significant.
Final passivation (PECVD nitride)	[K]	575	TBD	TBD	Other materials may be needed for non-hermetic packaging.
MOCVD (selective) regrowth	[K]	850 - 900	TBD	TBD	For spot size convertors, blocking layers and waveguides

Singulation	[unit]	2025	2030	2035	Comments
Facet definition		Cleavingetching	etching	etching	
Die singulation		cleaving	dicing	dicing	
Facet position accuracy	[µm]	5	0.5	0.05*	*Etched facet position limited by stepper overlay and etch profile control

PRIORITIZED RESEARCH NEEDS (> 5 YEARS RESULT)

As a major research priority, we consider the integration of photonics and electronics. The drive for higher performance and lower cost will require close integration of driver and control electronics with photonics. To reduce the cost of integration it has to be done at a wafer scale, either by hybrid or by heterogeneous integration. Understanding the performance requirements at the system level will drive the optimization of the integration platform and process (mechanical, thermal, reliability, etc.). This may likely need a holistic development approach or optimization, considering the performance requirements from the integrated system.

PRIORITIZED DEVELOPMENT & IMPLEMENTATION NEEDS (< 5 YEARS RESULT)

1. Epitaxy defect/particle density < 10 cm^{-2}. Fully automated epitaxial growth equipment
2. Dry etching - etch depth control <1% <20nm
3. Passivation reliability for non-hermetic packaging
4. E-beam mask overlay accuracy 10 nm
5. InP substrates TTV < 1 µm for scanners
6. Lithography resist selectivity (resist/etch, wafer TTV < 1 µm)
7. Etched angled facets for low-reflection coupling from and to beams normal to the chip edge (important for easy coupling to fibre arrays)

GAPS AND SHOWSTOPPERS

Crucial for the development of InP-based technology into high-volume technology with high yields is the development of improved equipment, as described in the sections ‘Critical (Infrastructure) Issues’ and ‘Technology needs’.

RECOMMENDATIONS ON POTENTIAL ALTERNATIVE TECHNOLOGIES

As a promising but also challenging technology for moving towards larger wafer sizes, we consider technologies for processing InP-based wafer stacks on silicon substrates. This requires bonding of unprocessed or partially processed InP wafers stacks on silicon or CMOS wafers, and removing the InP substrate. Integration on CMOS will require the epitaxy to be performed before bonding and develop a process flow compatible with CMOS line.

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