TEST TWG

Contents

Executive summary 1
Introduction 3
Roadmap of Quantified Key Attribute Needs 6
On-Wafer Testing 6
Bar / die testing 9
Life cycle testing (Mounted dies but also earlier)........10
Testing parameters of production processes........11
Situation analyses........ 19
Manufacturing processes 19
Design........19
Wafer level Testing........21
Bare die level Testing........22
Generic Photonic Device Testing........22
General Test Equipment 26
Critical (infrastructure) issues........ 26
Technology needs (related to Milestones) 28
Prioritized Research Needs 28
Prioritized Development & Implementation Needs........ 29
Design 29
Standardization of test metrics and qualification........29
Tools and methods........30
High throughput testing (sub second per chip)........31
Workforce development........ 31
Gaps and showstoppers 33
Standarization 33
Platform agnostic testing 34
Automation 34
High speed (rf bandwidth) testing 34
Optical testing for manufacture 34
User support........ 34

Analysis of testing results 35
Cost 35
Higher PIC technologies 35
Recommendations on Potential Alternative Technologies 36
Contributors 37

EXECUTIVE SUMMARY

In the electronic integrated circuit (EIC) industry, testing has become a mature process supported by practices and equipment that have been heavily optimized to drive down the cost and time spent on IC testing. In contrast, development of similar methods and tools for the photonic integrated circuit (PIC) community is still at an early stage and the extra complexity that arises from having to measure both in the optical and the electrical domain poses many challenges. In this chapter we define a number of key areas where development is needed and in each of these areas we strive to leverage as much as possible the existing knowledge, practices and infrastructure from the EIC industry.

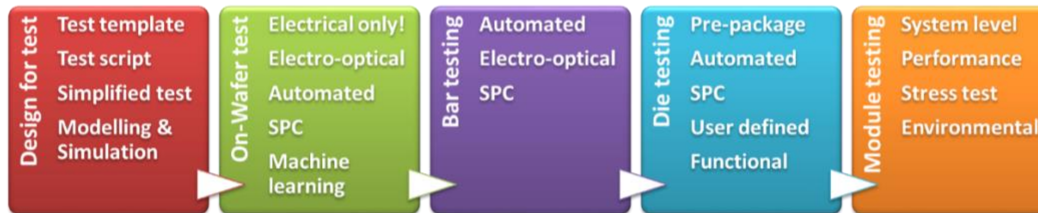

Figure 1. Overview of the test processes across the manufacturing chain of photonic integrated circuit based modules. Statistical process controls (SPC) require adequate test methods and data collection plans which should be accounted for already at the design phase.

The term PIC refers to an immensely diverse field of different implementations where we need to consider different (1) materials (InP, GaAs, Si, polymer, Triplex, glass), (2) integration schemes (monolithic, hybrid, etc.), (3) packaging (hermetic, non-hermetic, material) and (4) optical couplers (gratings, edge, mirrors coupled to single fibers, fiber arrays, lensed fibers, etc.). This leads to a first key development area: standardization of test metrics. New standardized testing methodologies and qualification parameters need to be devised that apply to all technologies, types of packages, and all relevant environmental conditions – leading to a truly platform-agnostic test solution.

A second focus area is to consolidate the design and test workflow (see example in Figure 1). A four-step method is proposed to enhance collaboration between designers, fab engineers and test engineers. Variations in dimensional and physical properties of materials and modules need to be understood and taken into account during design. This permits engineers to predict the influence of process variations on measurement results and allows them to design dedicated and improved test structures up front. By repeating these steps in combination with a careful analysis of the stored data, the number of devices to be measured and tracked can be reduced and the functional yield is expected to increase.

This targeted reduction in number of devices brings us to a third key area: test time reduction. There is a clear need for fully automated test systems. On the one hand this includes inline and where possible in-situ process testing at wafer level such as critical-dimension (CD) monitoring, defects counting, ellipsometry, etc. On the other hand, this includes the (out-of-line) automatic functional testing at wafer, bar/die and module level. For the functional test a massively parallel test approach is envisaged in order to bring down measurement time and cost.

More specifically for wafer-level testing, this highly parallel test approach can be enabled by scalable and modular test equipment and an increase in the number of electrical and optical input-output (IO) ports per test site. For electrical measurement instrumentation this modular approach is already quite well established; for optical instruments this is an emerging concept. In order to increase the number of optical IOs per test site from 10s to 100s of couplers in the next 10 years, multi-core fibers or fiber arrays will have to be used in combination with an optical interposer to reduce the pitch of optical IOs. Measuring optical signals indirectly using on-chip photodiodes is another interesting option to eliminate the need for optical alignment.

In contrast to silicon photonic (SiPh) chips, InP- and GaAs-chips often require bar /die level testing. Main reason is that often cleaved facets with ultra-low antireflection coating is needed for full device operation. In the future the target will be to replace cleaved facets by on-wafer etched facets and to replace facet coating by on-wafer coating. Then most of the bar / die testing can be avoided and wafer level testing can be used. In case of SiN devices it is expected that also in future die testing will play an important role.

In addition to functional testing, also the area of reliability / lifetime testing needs to be addressed. To date commercially available life time testing equipment is mainly based on fiber attached mounted single dies or mounted single devices that are being tested with free space measurement setups (e.g. laser lifetime measurements using large area photodiodes). Such investigations therefore cause high costs. Performing these tests at wafer level, simultaneously on multiple dies is an option to be investigated. This will also require developments in terms instrumentation, e.g. high-power laser sources for accelerated lifetime testing.

The IPSR-I Test TWG addresses overall lifetime test issues resulting from the inclusion of photonic capabilities into devices and products. Its emphasis is on wafers and dies with photonic functionality and assemblies and products that include these devices. Systems in Package (SiP), assemblies and bulk systems are addressed to the extent viable given the diversity of test needs that are specific to applications. As shown in Figure 2, the test issues for wafers, die, SiP, and systems will be addressed at the Design, Qualification, Validation, Production, and In-Use stages of product life cycles[1]. Current and anticipated optical parameters to be tested and their value or level are considered along with the test access issue at each stage of the product life cycle.

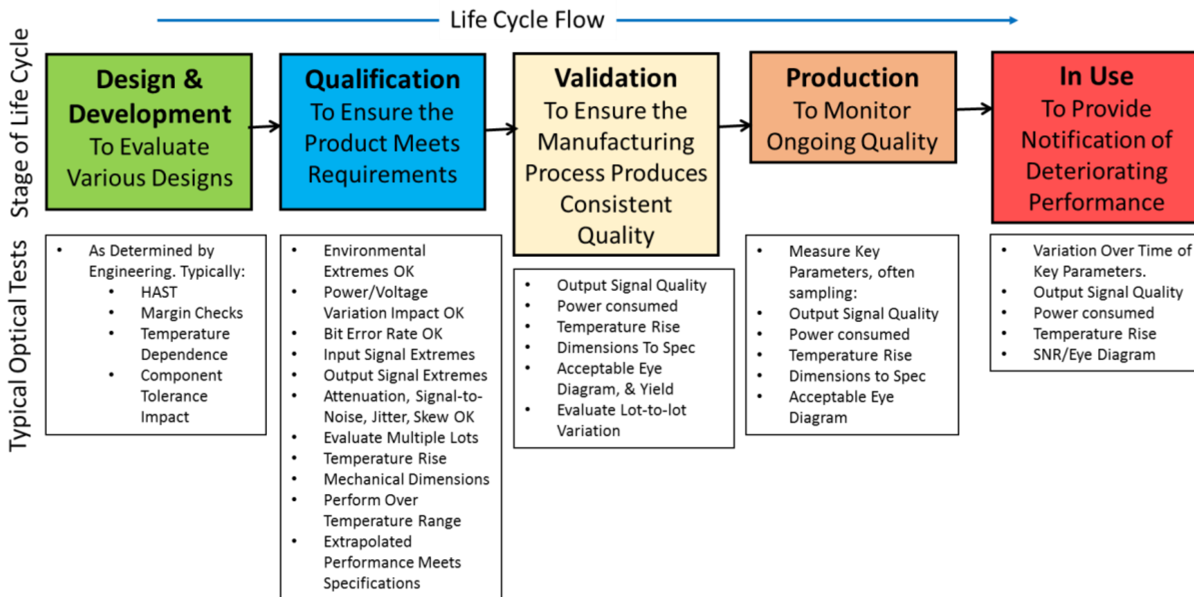

Figure 2 Test Needs During an Optical Product Life Cycle

[1] Testing and evaluation during Photonic Integrated Circuit (PIC) fabrication is specifically excluded and left for the Monolithic Photonic Integration chapter.

Telecommunications test equipment, components, and methods were and are being adopted for optical testing of products used for non-long haul applications. The traditional methods are being extended and new methods developed to address test needs for photonic wafers, photonic integrated circuits, and SiP that utilize optics and complete systems. Utilizing these extended methods requires optical probing of both wafers and dies combined with electrical probing resulting in a series of mechanical issues. The inclusion of optical probing, especially single mode probing, requires gratings or other access points on wafers. For individual die, dual mode (electrical and optical) probing is especially difficult due to the small size of die and difficulty of holding and locating probes accurately. At the SiP level, the problems are easier because the device is larger, not as fragile, and is often designed to facilitate dual media probing. The wafer, die, and SiP probe fixtures tend to be expensive due to the complexity and accuracy required. System level test access is usually easier because at that level, electrical interfaces and optical connectors are included as part of the device under test (DUT).

In addition to probe access, optical test methods to simultaneously characterize and compare multiple optical lanes, channels and/or ports at the same time are needed. One need is comparative simultaneous testing of multiple signals from arrays of ribbon fibers, waveguides, sources or detectors for optical skew, jitter, etc. A related need is to simultaneously evaluate optical signals multiplexed on one fiber or waveguide. Applications with arrays exceeding 256 ports (fibers or waveguides) or >256 multiplexed wavelengths are forecast in the next ten years.

In addition to the standard telecom optical parameters such as power, wavelength, attenuation, jitter, signal-to-noise ration (SNR), etc., emerging applications aim to utilize virtually every parameter that light can have, potentially requiring the extension of test capability in multiple dimensions such as polarization, phase noise, amplitude noise spatial modes, multiple fiber cores, etc. While these emerging needs are potentially very broad, the near-term emerging needs seem most likely to be extensions of data communications needs.

Optical communication applications are likely to utilize 650 nm to 2000 nm wavelengths, multiplexed wavelength spacing down of 25 GHz, detector responsivity of ~1 A/W, receiver sensitivity as great as -45 dBm, power levels of 1 Watt or less, symbol rates of 100 Gbaud per lane, modulation schemes utilizing up to 10 bits per symbol, polarization multiplexing, BERs of 10^{-12}, etc. Over time, these parameters will improve so test capabilities will need to stay ahead of them. Data rates as high as 500 Tbps per fiber are likely to emerge in the next 10- 15 years.

Sensor applications are likely to grow significantly in the next 10-15 years as remote fiber sensors are integrated into physical structures for strain and temperature sensing, and as chip-level chemical and biological sensors are introduced into the marketplace. While these applications will still require the same baseline test solutions as is required for telecom and datacom, the functional tests are likely to be quite different.

Quantum technologies add yet a different dimension for testing. The use of single photon and entangled-photon sources and circuits will yield its own complexity. There is currently no standardized test equipment for these applications; however, testing methods are currently being developed with University, Government, and Industrial research labs and will require consideration in future editions of this document.

REGARDLESS OF APPLICATION, THE PRINCIPLES OF *DESIGN FOR TEST* REMAIN THE SAME: THE USE OF OPTICAL TEST ACCESS POINTS, BUILT-IN SELF-TEST (BIST), REDUNDANCY FOR SELF-REPAIR, RE-PURPOSE AND PROGNOSTICS TO REPORT CHANGES AND DETERIORATION DURING OPERATION OVER THE LIFE CYCLE OF OPTICAL PRODUCTS ARE DESIRABLE AND OF VALUE IN AN INCREASING NUMBER OF APPLICATIONS. THESE TESTS SHOULD BE CONSIDERED FOR INCLUSION NOT ONLY IN DESIGNS, BUT ALSO IN SOFTWARE DESIGN TOOLS AS WELL.

INTRODUCTION

The Test chapter focuses on unique attributes of testing optical devices. No attempt has been made to duplicate required and typical electrical or mechanical testing. The chapter is open ended on optical applications testing with much of the material broadly applicable. It does, however, concentrate primarily on testing data communications products.

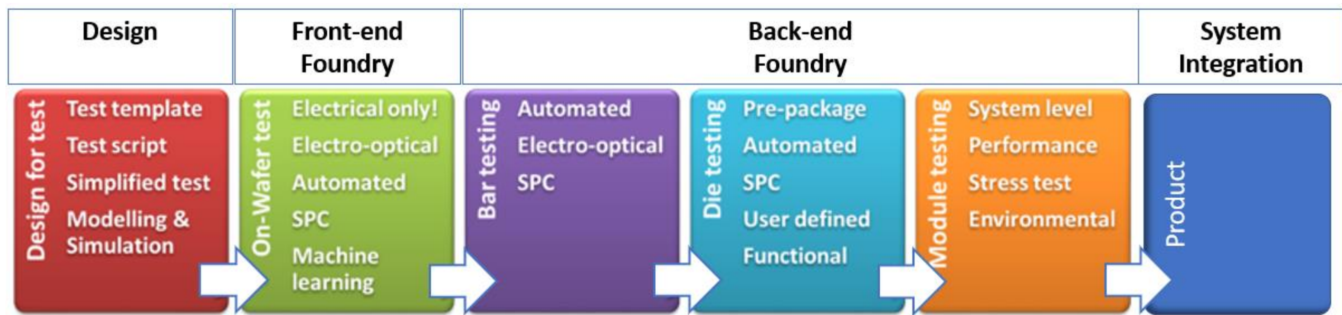

Figure 3 An overview of the PIC production chain for test.

In each step of the test chain that is followed by the components that will form an end product different requirements and methods are used. This chapter will discuss both the separate steps, as the connection between those steps regarding the product and data flow.

Areas of testing need during a product life cycle are:

a. during development to prove functionality and de-bug devices
b. qualification testing
c. pre-production validation
d. in-process production testing to assure product quality, reliability and to improve yield.

This chapter contains an overview of PICs made on InP, SiN, SiPh, GaAs, Polymers and CMOS platforms. Elements like fiber couplers, fiber arrays, lenses, optical and electrical interconnects and the standardization of test port positions (optical, DC, RF) will also be discussed.

The kinds of testing required vary over the life cycle of a product (Figure 2). Test Needs during an Optical Product Life Cycle lists typical optical device test activities and requirements during the life of a device from conception through the in-use and end of life phases.

Lanes vs Channels

An optical lane utilizes one wavelength traveling from one point to another in one fiber or waveguide. Information may be imposed on the beam utilizing any methods such as On-Off-Keying, PAM XX, dual polarization or any method that effects only that wavelength.

A Channel may consist of a single lane but often, even usually, has multiple lanes. The lanes may be on multiple parallel fibers or waveguides, or on the same fiber or waveguide utilizing wavelength division multiplexing. Many datacom standards utilize multiple lanes to achieve their data rates.

Evaluating technical capability is most easily done utilizing lanes because channels that combine many lanes make it difficult to understand the underlying technology. System designers, however, find the channel view more useful as the technology details are not important at their level.

Prescriptive Starts Here

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS

ON-WAFER TESTING

Ideally, the estimation of the yield of a wafer for a particular PIC product occurs on-wafer at the final stage of the fabrication. This way, the number of handling steps can be reduced, and even eliminated (such as the handling of the bars during the bar-level tests). On-wafer electrical- and optical testing is possible for PIC products by introducing the grating couplers and/or vertical mirrors into the PIC fabrication process. As a result, the grating couplers and/or vertical mirrors on the wafer need to be coated on wafer level, and the electrical measurements have to be done in a pulsed-mode operation (preferably with standardized pulse widths). Therefore, for those PIC products that do not require endface coupling, this solution is ideal in that all the relevant testing from PIC performance, to far-field measurements of the grating couplers/vertical mirrors can be done in a straightforward manner.

Most optical measurements of devices such as measurement of optical waveguide losses require the use of vertical in/out grating couplers or angled mirrors. Furthermore on-wafer facet coating of all devices will be needed to significantly reduce all bar and die measurements. For the electrical wafer testing mature electrical tools will be used. The amount of I/O will increase in future. Today typically 4 and 16 I/O are used:

Table 1 On-wafer testing

	[unit]	2020	2025	2030	2035	2040
# of Optical I/O	per chip	16	32	64	128	256
Pitch of Optical I/O	µm	256	127	65	20	15
Optical I/O Geometry		Linear Array	Stacked Linear Array	Small diameter or multicore fiber	Multicore fiber	Multicore fiber

By use of fibre arrays, multicore fibres or different multiple I/O optical probe technology a parallelization of the measurements will be achieved in future. To this end, standardized input/output gratings couplers will be used to match the chosen optical probe technology. On the other hand, such measurements will be possible only if suitable modular and scalable measurement equipment is available, e.g. mutli-channel and fast high power tunable laser sources, multi-port power meters, polarization controls, optical switch matrixes,

The following tables summarize the current status and the expected development of the device testing within the next 15 years. Laser diodes (LD), photo-detectors (PD) and Mach–Zehnder Modulators (MZM) are considered for different fabrication technologies as applicable: and Table 2 for silicon, Table 3 for InP and GaAs and Table 4 for SiN.

Table 1 Wafer level high throughput testing -Si-Photonics

<table>
<tr><th>Wafer level high throughput testing - Silicon-Photonics</th><th>[unit]</th><th>2020</th><th>2025</th><th>2030</th><th>2035</th><th>2040</th></tr>
<tr><td>Propagation loss
ex. Si-wire, polymer, and rib waveguides
(measure some waveguides per chip)</td><td>[dB/cm]</td><td rowspan="3">30 min/chip
Semi-automated</td><td rowspan="3">5-20 min/chip*
Fully automated</td><td rowspan="3">5-10 min/chip with
2-4 probes

(1-5 min/2-4 chips)</td><td rowspan="3" colspan="2">2-5 min/chip
multi 4-8 probes

(0.5-2 min/4-8 chips)</td></tr>
<tr><td>Insertion loss
ex. modulators (measure some devices per chip)</td><td>[dB]</td></tr>
<tr><td>Spectrum (Operating wavelength)
ex. Grating couplers, Directional couplers, Ring resonators
(measure some devices per chip)</td><td>[dBm/nm]</td></tr>
<tr><td>Contact resistance</td><td>[Ω cm^2]</td><td rowspan="2" colspan="5">use current/mature electrical tools</td></tr>
<tr><td>Sheet resistance</td><td>[Ω/sq]</td></tr>
<tr><td>$V\pi$ L or (Vpi)
ex. MZI/Ring switch (heater), MZI/Ring modulators (pin/pn junction)</td><td>[V cm (or V)]</td><td rowspan="7">20 min per device or circuit
semi-automated</td><td rowspan="7">10 min per device or circuit
semi-automated</td><td rowspan="7">5 min per device or circuit
fully automated</td><td rowspan="7">2 min per device or circuit
fully automated</td><td rowspan="7">1 min per device or circuit
fully automated</td></tr>
<tr><td>f_{3dB} (EO bandwidth)
ex. MZI/Ring modulators</td><td>[GHz]</td></tr>
<tr><td>Responsivity
ex. Ge photodiode</td><td>[A/W]</td></tr>
<tr><td>Dark Current
ex. Ge photodiode</td><td>[nA]</td></tr>
<tr><td>f_{3dB} (EO bandwidth)
ex. Ge photodiode</td><td>[GHz]</td></tr>
<tr><td>Eye pattern
ex. MZI/Ring modulators, Ge photodiode</td><td></td></tr>
<tr><td>BER (Bit Error Rate)
ex. MZI/Ring modulators, Ge photodiode</td><td></td></tr>
<tr><td>environmental testing
ex. temperature -40 to +85 ℃.</td><td></td><td colspan="5">Adapt current/mature environmental tools</td></tr>
</table>

* not including wafer load/unload time (Front Opening Universal Pod (FOUP/Front Opening Shipping Box (FOSB) to testing state to FOUP/FOSB).

Table 3 High throughput testing of InP and GaAs devices

Parameter	Unit	Test Level	Test Time Goal
output power – laser diode (LD)	[mW]	bar level	1 min/device
threshold current LD	[mW]	bar level	
SMSR LD	[dB]	bar level	
RIN LD	[dBc/Hz]	bar level	
Frequency noise spectrum LD	[Hz^2/Hz]	die level	
Frequency response LD	[GHz]	die level	
Extinction Ratio LD	[dB]	die level	
Sensitivity MZM	[$V_{2\pi}$]	bar level	2 min/device
Modulation bandwidth MZM	[GHz]	bar level	
Insertion loss MZM	[dB]	bar level	
Responsivity PD	[A/W]	wafer level	1 min/device
Bandwidth PD	[GHz]	wafer level	

Table 4 Wafer level Inspection- SiN devices

Parameter	Unit	Test Level	Inspection Time Goal
Layer stack quality	Particle density	Experienced eye	5 min
Lithography quality	Resolution test & defect count	manual	5 min
Etching quality	Compare with litho check	Microscope manual	5 min
Top cladding quality	Visual defect check	Microscope manual	10 min
Actuator check	Visual defect check	Microscope manual	5 min
Wafer level bump check	Visual defect check	Microscope manual	10 min

BAR / DIE TESTING

In contrast to Si-photonic the InP- and GaAs-chips often require on bar /die testing (see table below).

Main reason is that often cleaved facets with ultra-low antireflection coating is needed for full device operation. In the future the target is to replace cleaved facets by on-wafer etched facets and to replace facet coating by on-wafer coating. Then most of the bar / die testing can be avoided and wafer level testing can be used.

In case of SiN devices it is expected that also in future die testing will play an important role.

Table 2 Bar/die testing InP and GaAs devices distinguishing serial (single device at a time) and parallel testing.

	[unit]	2020	2025	2030	2035	2040
output power LD	[mW]	serial	parallel	parallel wafer level test		
threshold current LD	[mW]	serial	parallel	parallel wafer level test		
SMSR LD	[dB]	serial	parallel	parallel wafer level test		
RIN LD	[dBc/Hz]	serial	parallel	parallel wafer level test		
Frequency noise spectrum LD	[Hz^2/Hz]	serial	parallel	parallel wafer level test		
Frequency response LD	[GHz]	serial	parallel	parallel wafer level test		
Extinction Ratio LD	[dB]	serial	parallel	parallel wafer level test		
Sensitivity MZM	[$V_{2\pi}$]	serial	parallel	parallel wafer level test		
Modulation bandwidth MZM	[GHz]	serial	parallel	parallel wafer level test		
Insertion loss MZM	[dB]	serial	parallel	parallel wafer level test		

Table 3 Die testing SiNx-devices

Die testing SiNx-devices	[unit]	2020	2025	2030	2035	2040
Waveguide defect check	# defects/chip % of defect chips yield	End facet incoupling of light and VIS & IR monitor on top of chip-Manual place, Auto align. Operator required.	Auto place & align and auto record. No operator. Manual analyze. Obtain statistics.	Full automation of acquisition and analysis		
Waveguide loss check	dB/ cm, loss spectrum	Manual place & Auto alignment to loss test structures.	Auto place & align & auto measurement. No operator. Manual analyze.	Auto place Auto align & measure Auto analysis		

		Operator required.	Obtain statistics.	
Building block test (DC, MMI, RR, MZI)	Insertion loss, splitting ratio, FSR,	Manual place & Auto alignment and measure. Operator required.	Auto place, align & auto measurement. No operator. Manual analyze. Obtain statistics.	Auto place Auto align & measure Auto analysis
Actuators	# Defects / chip Sensitivity ($V_{2\pi}$)	Manual place & Auto alignment and measure Operator required	Auto place, align & auto measurement No operator. Manual analyze. Obtain statistics.	Full automation of acquisition and analysis

Life cycle testing (Mounted dies but also earlier)

To date commercially available life time testing equipment is mainly based on fibre attached mounted single dies or mounted single devices that are being tested with free space measurement setups (e.g. laser lifetime measurements using large area photodiodes). Such investigations therefore cause high costs. For some of the test conditions (e.g. high temperature, high humidity) it is not clear how the materials (e.g. epoxies) used for fiber attachment will behave, so we actually need to study (1) the reliability of the fiber attachment and (2) reliability of the opto-electrical components and make sure one reliability aspect does not affect results for the other.

In future a parallelization of these lifetime measurement will be tackled, operating a large number of devices on wafer scale at the same time avoiding the mounting of single dies. As to the testing of e.g. photodiodes or waveguides high power laser sources are needed (especially considering parallel testing and thus splitting the laser output over multiple channels). However, for lifetime testing of the devices including the mounting / bonding process, testing on die level will be required.

Table 7 Life cycle testing InP and GaAs devices

Life cycle testing InP and GaAs devices	[unit]	2020	2025	2030	2035	2040
Optical output power	[mW]	established				
Threshold current	[mA]	established				
Optical wavelength	[nm]	none	started	established		
SMSR	[dB]	none	started	established		
Responsivity	[A/W]	none	started	established		

Testing parameters of production processes

To guarantee stable and high yield production processes it is a stringent requirement to test a large variety of different processing parameters while processing the wafers. These parameters to be checked still strongly depend on the devices fabricated. However, with view to a steadily increasing monolithic integration depth the parameters to be checked per wafer will converge in future.

The most important processing parameters to be checked during the processing are:

- etch depth uniformity: nm resolution, over 1 micrometer etch depth
- waveguide sidewall roughness: sub nm resolution, over 1 micrometer depth
- layer thickness and refractive index: 1*10-4 accuracy, versus speed of measurement
- waveguide width measurements: nm resolution
- resistance measurements of heaters
- conformal filling measurement
- photoluminescence: micrometer resolution
- particle analysis
- imbalance in coupler structures (trimming possible)
- atomic force microscope to determine grating depths (trimming possible)
- resist thickness and structure width
- doping levels

Furthermore, several components can be measured during the wafer processing before finalizing it. This characterization can be done by electrical/optical probing:

- photodiodes
- lasers
- heaters
- separation / isolation resistance

Table 8 Testing production processes polymer devices

	[unit]	2020	2025	2030	2035	2040
Dimensions (line width, hole diameter)	[nm]	1 nm (use mature CD SEM tool)				
LER (Line Edge Roughness) *1	[nm]					
Film thickness	[nm]					
Alignment precision of lithography (especially, pn ion implantation for optical modulator)	[nm]	Use mature optical overlay equipment				
Passive optical properties *2 Propagation loss	[dB/cm]		5-20 min/chip Fully automated	5-10 min/chip (parallel) 2-4 probes (1-5 min w/2-4 chips)	2-5 min/chip (parallel) 4-8 probes (0.5-2 min/4-8 chips)	
Insertion loss	[dB]					
Spectrum	[dBm/nm]					
Qualification of polymer materials	°C	Manual	Manual	Automated		
Active and passive polymer curing, poling, Teng-Mann testing control		Manual	Manual	Automated		
Poling measurements		Manual	Manual	Automated		
Electrical probe and contact to polymer materials		Manual	Manual	Automated		
EO polymer r33 performance (EO activity in material)	pm/V	Established	Mature	Mature		

*1 LER: Si top LER can be measured, but side wall roughness cannot be measured directly.
Correlation between CD SEM and optical properties should be investigated using image analysis and empirical approach.
*2 Contactless and non-destructive inline optical testing (with no particle pollution)

Table 9: Testing production processes InP and GaAs devices

	[unit]	2020	2025	2030	2035	2040
etching depths	nm	Established				
waveguide width	nm					
resistance measurements	Ω					
on wafer facet coating reflectivity	%	No current capability	No planned capability	Planned Capability	Implemented	Establis hed
thickness and refractive index of deposited dielectrica	nm	Established				
thickness of overgrowth layers	nm					

A projection of the key industry needs is shown in Table

Table 10 Key challenges with respect to test between 2020 and 2040

	2020	2025	2030	2035	2040
Adopt semiconductor EIC industry test practices					
Test procedures from custom to standardized					
Standardization of test structures					
Test data exchangeability and analysis					
Technology agnostic testing					
Test automation					
Design for test					
Application agnostic testing					

Red: Not current industry practice; Orange: Partial industrial coordination; Yellow: Significant industrial coordination and compatibility; Green: Established Industry standard.

Each category is broken down in more specific subcategories in the following tables, following the same roadmap guidelines. Each table addresses areas such as key challenges, test practices, transition from custom to standardized procedures, transfer of data, adopting semiconductor test practices, design for test both at the die level and the software level. The tables show competences going out beyond 5 years and emphasize relative strengths for each area.

Table 11: Adopt semiconductor EIC industry test practices

	2020	2025	2030	2035	2040
6 Sigma methodology					
Documenting and reporting					
The same metrics but methods may vary					
Optimized test at wafer-level					
DC testing in electrical – electrical domain					
Revised accept-reject methodology					

Table 12 Transition from custom to standardized procedures.

	2020	2025	2030	2035	2040
Standards instead of custom approaches					
Prioritize tests across full PIC value chain					
Testing metrics					
Relevance of a test					
Standardized test structures					

Table 13 Transfer of test data across the PIC value chain

	2020	2025	2030	2035	2040
Implementation in PDK **Improved design tools (EPDA)**					
Correlation of the test outcomes **Improved processes** **Identification of redundancies**					
Accessible scope – potential IP issues					

Table 14 Technology agnostic testing

	2020	2025	2030	2035	2040
Across (currently) major technologies InP, SiPH SiN, Electro-Optic (EO) polymers					
Open for emerging platforms polymer, diamond, rare earth ion doped, three-dimensional (3D) PICs, SoC (high temperature)					
Hybrid integration photonic cross platform electronic-photonic chip level (EPICs) electronic-photonic PCB-chip					
Testing PICs with CMOS circuits/testing					

Table 15 Automation of test at wafer, bar, die, module and system level testing

	2020	2025	2030	2035	2040
Wafer - level					
Bar and die – level testing					
Standard test interfaces (layout templates)					
Technology agnostic					
Scalability					
On-chip self-diagnostics (Utilizing electrical-to-electrical testing)					

Table 16 Design for test

	2020	2025	2030	2035	2040
Test oriented layout templates					
Implementation in PDKs					
Test scripts for generic die testing					
Training of PIC designers					

SITUATION ANALYSES

MANUFACTURING PROCESSES

Design

Testing is a time consuming and complex task, and a significant contribution on the final cost of a device, but essential at different stages in the development of a photonic integrated circuit. Testing aims to verify fab process tolerances, validate foundry manufacturing, extract building block parameters, and analyze system level performance of overall circuits. Since there is a sheer variety of PIC designs, it is very complicated to have a generic or application independent testing procedure.

Testing starts at the design stage. On one hand, foundries design their own test cells for process control monitoring (PCM), containing specific structures to verify and validate the wafer fabrication, ensure basic building block performance, obtain statistics for PDK maturing, and estimate yield. On the other hand, designers should also include *smart* and *proper* test structures in their designs, not only to ease the testing task later on, but to verify complete design functionality, extract additional parameters, and to corroborate data provided by foundries. However, there are currently no standards for these test structures, so it usually depends on the designer’s experience and proper communication with testing engineers.

In a view of the PIC production chain as depicted in Figure 3 after the design stage, actual testing can be divided into a number of categories: wafer level, bar level, bare die level and package level.
There are three main drivers to develop integrated photonic solutions, particularly in telecom and datacom applications. The first driver is the cost of integrated photonics modules tracks much closer to the cost of traditional electronic ICs and are a fraction of the cost of the traditional optical solutions. The second driver is that Integrated Photonic modules are also much lower power and smaller. The third driver is that, integrated photonic modules offer much more in terms of scaling towards ever growing demand for bandwidth and speed.

Commercial companies ar e designing and manufacturing integrated photonics modules for all of the above reasons. Companies must be able to sell these modules, whilst maintaining acceptable profit margins as expected by the financial markets. To obtain these margins, yields need to be high and the cost of test low. This applies to the cost of test equipment for both validation and production.

The end to end cost to manufacture, assembly and test of a complete integrated photonic module must be taken into account, when designing the PIC, the electrical ICs and picking the composite components. Thought needs to be given to how much electrical testing can be done, that will predict the functioning of the optical waveguides, and whether there are optical wafer acceptance test parameters that will also predict functioning devices.

An automated test equipment (ATE) for optical solutions is difficult and expensive to implement and may not well represent the performance of the final integration of a laser and other components into the modules. For example, if the electrical testing of the PIC can be 95% accurate to predict good die, the cost calculation may show that it is actually cheaper to throw away bad modules built with the 5% bad die, than to pay for ATE for optical test. It is recommended that commercial photonic companies do an end to end cost and yield analysis of each test step vs the cost of test equipment to understand the most cost-effective test solutions.

It is very important to keep the data collected across the production chain into account during the design phase and the complete process as depicted in Figure 4. Test results are collected and analyzed by designers and manufacturing engineers at each individual step. Although the nature of test at each step differs a data flow allowing for open exchange between all stages is crucial for development of correlations and optimization of test processes.

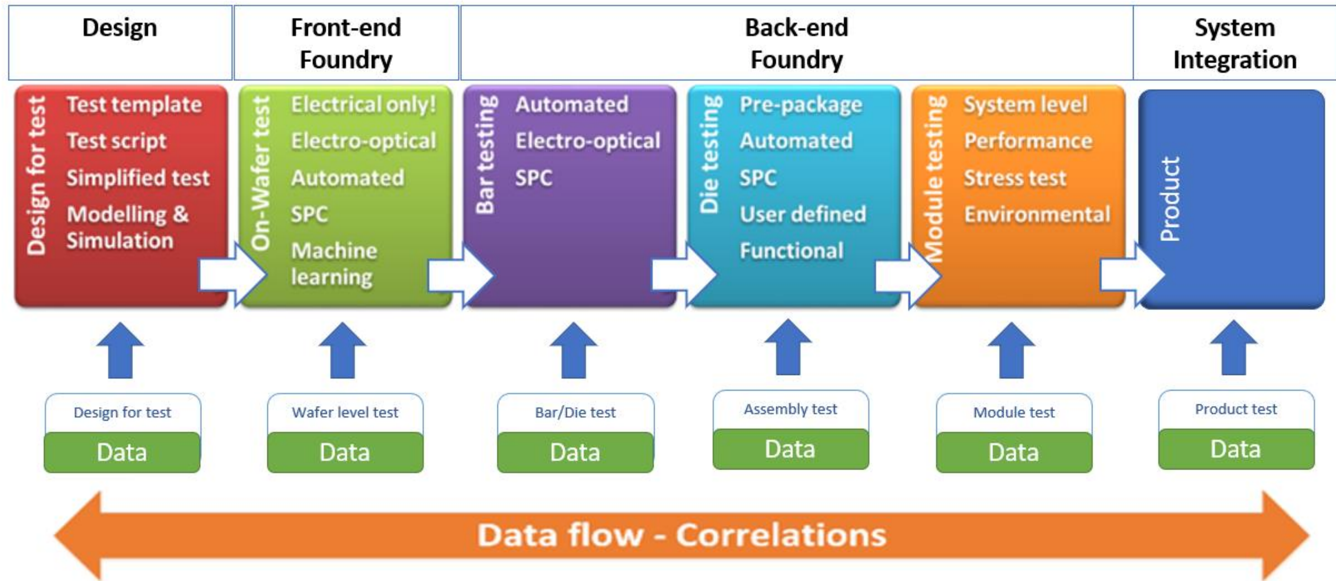

Figure 4. Test framework for data flow and exchange across production chain from a design to product (www.openepda.org).

Test frameworks (www.openepda.org) utilizing open standards assure data interoperability, exchangeability and traceability, inherently enable such data flow. Such test framework is hardware agnostic and can be deployed around any tool and equipment configuration. It decouples operators from low-level hardware control, allows for dynamically adjusted test sequences and customized analysis modules. Machine learning techniques may further augment the capabilities of such an approach by increasing efficiency of data analysis and decision making.

The demand for test differs at different development stages of the manufacturing process as suggested in Figure 5(a). It is particularly important at initial start-up phase and changes as the manufacturing process develops. The rate of this change is different at each phase and is inversely proportional to the yield. The cost of test is proportional to the product of the number of items tested, frequency of test events and the production volume. Also, since the cost of test must be borne by the passing devices, the cost of test per good-device goes up significantly as the yield drops (Figure 5 (b)). The long-term cost of test trend follows the demand for test and gradually decreases as the manufacturing process matures.

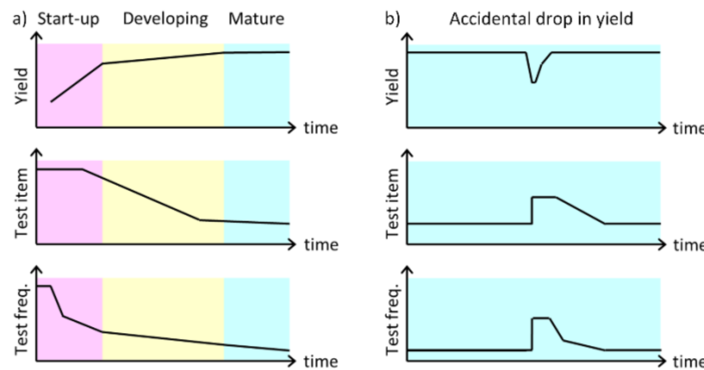

Figure 5. (a) Demand for test at different development stages of production process over time in perspective of yield, number of tested items and frequency / number of test cycles of test events. (b) Disruptive event in yield with an impact on number of tested items and test frequency.

In order to manufacture efficiently, certain level to test for screening has to be considered and put in place at different points of production chain, as presented in the Figure 6.

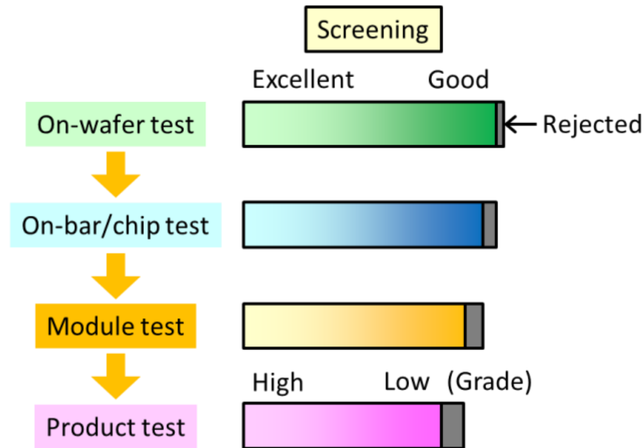

Figure 6. Test for screening is essential to manufacture products efficiently.

The wide spread of test processes across the full production chain results in massive test data being collected in the manufacturing process. Test strategy for keeping high yield, screening, etc. is determined based on such massive test data and it is very important to establish the best test strategy. This will remain challenging because the best test strategy varies in each situation.

Wafer level Testing

Wafer testing is mainly carried out by front-end foundries and test houses, and provide both, visual and electrical and/or optical testing.

Within the foundry, during wafer manufacturing, both visual inspection and quantitative measurements are performed at each step in the fabrication process. The primary goal here is to examine the wafer for irregularities in the process. For example, film thicknesses, etch depths, and line widths can all experience process variations. Most of these measurements are part of the standard suite of inspection methods for electronic ICs. The visual inspection is still manual much of the time and is usually executed only in limited regions of the wafer, requiring machine vision systems providing enough resolution, multi axes positioners and capability to inspect different wafer sizes and materials. Once the fabrication process is complete, and before singulation, final wafer metrology is carried out.

Optical microscopes are useful for obtaining physical dimensions of the fabricated structures, layer thicknesses, surface roughness, and (for III-V materials) can also create photoluminescence maps, giving information of material composition and quality, bandgap determination, etc. Modern digital microscopes have sophisticated stitching and profilometry algorithms that can provide an accurate picture of trench depths, and waveguide path accuracy over relatively large areas.

Scanning electron microscopy (SEM) testing has always been important technique at the wafer level. However, integrated photonics circuits add a level of difficulty to SEM testing because of the insulating oxide layers both above and below the silicon and silicon nitride waveguides. These oxide layers result in charging; without a conductive coating on the wafer surface, an oxide-coated PIC may yield a distorted image.

Since defects/irregularities detection at this early stage of the development will have a great impact on the final cost of PIC development, it would be necessary to develop test pattern-recognition algorithms for the visual inspection and metrology and formulate a pass or fail criteria depending on technology (InP, SiN, SiPh, etc) and structures.

At the wafer level, along with visual inspection and taking advantage of the pre-existing equipment for CMOS technology, electrical testing can also be carried out. As a matter of fact, at this level, electrical measurements are easier than optical ones, due to the fact that, at the wafer level, coupling light to, or extracting light from individual dies is a challenging task given the tight tolerances required. Electrical measurements can be carried out much faster and at lower equipment cost.

The straightforward approach to carry out optical tests is by means of vertical grating couplers. However, these structures can only be implemented in a few technologies (e.g. SiPh, SiN) and have limited spectral bandwidth. Thus, different structures/approaches have been proposed to overcome these limitations, such as: reflective 45º mirrors, evanescent coupling, etc., or by means of indirect electrical measurements (Contactless Integrated Photonic Probe, CLIPP) [2] when possible.

Even though, optical testing is still challenging. Wafer prober stations are difficult to interface with optical probes, so both need to be adapted/designed accordingly to the requirements, and this makes the resulting solutions not very flexible, increasing the throughput but limiting the re-usability for different applications.

Furthermore, optical probes require (semi-)automated alignment, with very high resolution.

Bare die level Testing

Ideally, foundries should provide both parameter values and their expected statistical variation to end-users; these are usually built into the parametric models used to describe each building block in the photonics process design kits. However, due to all of the challenges associated with optical testing at wafer level, bare die testing is still carried out to extract most building block parameters.

Bare die testing typically has low levels of automation and is therefore costly and complex. Thus, only a small subset of tests and structures are measured by the foundry, and it is up to test houses or end-users to carried out more complex, extensive characterization of individual building blocks, or system level functionalities of the overall circuit.

It is worth noting that many measurement procedures for PIC testing are not yet standardized. This is true both for testing of individual building blocks (sub circuits and devices) as well as for full, functional circuits. This often leads to a wide variety of test setups (leading to different measurement results) between foundries, test houses, designers, and end-users. Defining standards/procedures at this early stage of the technology may seem too ambitious, but instead what is proposed in the short term, is to define good practices.

Generic Photonic Device Testing

Figure 7 illustrates the general test requirement; the need for both electrical and optical test inputs, and then analysis of the electrical and optical outputs from the device under test (DUT). In addition, environmental parameters, such as temperature, humidity, vibration, etc. may be test inputs. Finally, in addition to the optical and electrical test responses, physical factors, such as temperature rise, may be outputs that are monitored during testing.

[2] F. Morichetti et al., "Non-Invasive On-Chip Light Observation by Contactless Waveguide Conductivity Monitoring," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 20, no. 4, pp. 292-301, July-Aug. 2014. doi: 10.1109/JSTQE.2014.2300046

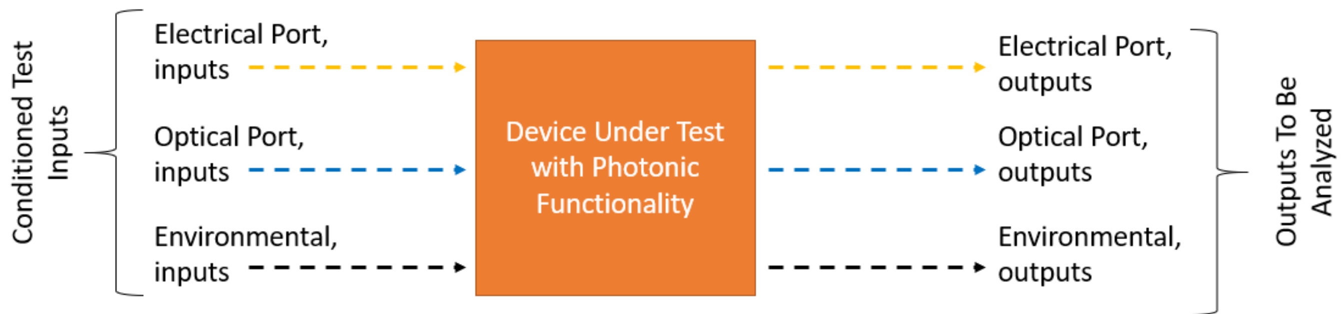

Figure 7 Generic Photonic Product Test Environment

The electrical ports are electrical contacts, or arrays of contacts, for power, control, monitoring of functionality, and, of course, data inputs and/or outputs.

The light directed to an optical input port may be in the form of one or more optical beams or it can be guided by one or more fibers. In either case, it is typical to arrange the parallel inputs in a regular array, the size of which must be considered in the PIC design. The light can either be a constant source (that is then modulated by the device under test) or it can carry a modulated data stream (if the intended function of the device is to de-modulate the data). The optical interconnections may be in the form of butt/edge coupling, a grating coupler, or an evanescent coupling resulting from proximity of parallel waveguides. Making these test connections, especially the optical connections, is frequently a major project.

The photonic input and output signals may have multiple parameters needing measurement. Specifically, optical signals may require measurement of the following properties of individual sources, lanes or channels:

- Power
- Polarization
- Direction
- Mode profile
- Wavelength
- Variation in any parameter (e.g. power, wavelength, polarization) over time
    - modulation (fast)
    - drift (slow)
- Skew between beams
- Component loss
- Return loss

System (functional) properties:

- Signal-to-Noise Ratio (SNR), Relative Intensity Noise (RIN), Phase-Noise, Crosstalk
- Bit error rate (BER)
- Variation of system figures of merit with temperature and other environmental inputs

A typical measurement requires a source with a means of controlling one or more of these parameters. The source will typically be coupled into a single mode fiber that, for some systems, must be polarization maintaining. The source can be tunable (in cases where the wavelength dependence is part of the measurement), narrowband (for monochromatic measurements) or broadband in certain sensors applications. The light is injected into waveguides via optical ports and routed (according to the PIC design) through one or more active or passive components. Active components typically require one or more electronic drive signals. These components (the devices under test) will modify the input optical signals in a manner determined by the magnitude, phase, and frequency of the electrical drive signals. The resulting electrical and optical signals are on the corresponding output ports.

Environmental inputs may include all of the usual variables: temperature, humidity, temperature cycling, Highly Accelerated Stress Test (HAST), vibration, shock, etc.

Physical outputs include temperature rise, mechanical changes such as delamination, cracking, swelling, wire breaks or optical chain interruptions, etc.

Photonic test requirements vary by the test level (wafer, die, photonic SiP, system) and test need (access, sources, detectors, functions). Table 17, Photonic Test Requirements gives a generic view of the testing needs for items containing photonic elements at the various levels.

A similar table can be developed for specific applications to provide some insight into the related requirements for each application.

Table 17: Photonic Test Requirements

	Test Need			
Test Level	**Optical Access**	**Sources**	**Detectors**	**Functions**
Wafer	45° mirrors, vertical grating couplers, etched factes, cleaved fiber, tapered fiber, lensed fiber, focused free-space beam, evanescent coupling	External sources injected via fiber or free-space access Integrated sources	External photodetectors, potentially in arrays; Imaging sensors Optics to collect and/or image light to be detected. Integrated photodetectors	Wide variety of device characterization and functional tests; media loss/cm, insertion loss, modulation depth/bandwidth, polarization control, wafer uniformity, detector sensitivity/responsivity, temperature sensitivity, die-to-die variation, skew between outputs
Chip	The same as wafer options plus edge coupling to embedded or surface waveguides.	The same as wafer options	The same as wafer options	The same as wafer options plus edge coupling impacts on loss, spectral bandwidth and polarization
Photonic SiP	Butt coupling or expanded beam connector, evanescent coupling, fiber splice, ribbon fiber splice	External or on-chip laser source to simulate application related requirements.	External detector or detectors, potentially in an array, gathering light from an edge emitting waveguide or vertical emitting 45° mirror, or vertical emitting grating	The same as wafer and chip options, plus characterize package connections, and application specific tests such as eye diagrams, BER, environmental sensitivity
System	Conventional optical connector, fiber splice	External or internal laser source or sources to simulate inputs.	As needed to measure and evaluate system outputs.	Intensity, skew between lanes, polarization, eye diagram, SNR,
In Use, Over Lifetime	Limited, if any. System dependent access.	Both self and remotely initiated data reporting	Primarily wireless or electronic	Monitor & report performance changes. Initiate self-repair.

Several types of product testing of devices, including those with photonic capability, usually are required:

- Test during development to ensure the design “works”
- Qualification testing, typically done before a product is committed to wide use
- In-process testing to monitor manufacturing process quality
- Final testing before each individual product is shipped to a customer

GENERAL TEST EQUIPMENT

Optical device test equipment is available from multiple suppliers. Historically, the telecommunications industry was the major consumer, but in recent years the use of optical communications for short distances, such as Local Area Networks (LANS), Fiber to the X (Home, Office, Curb, Node, etc.) (FTTX), and Active Optical Cable (AOC) and in Data Centers, as well as a variety of sensors, has broadened the demand. Much of the demand emerging for these new optical applications is filled by utilizing equipment developed for and derived from that used by the Telecom sector. As these applications grow in importance, specialized equipment is emerging and becoming available.

Devices under test can vary dramatically, so defining all the needed instruments for PIC testing is not the most appropriate approach. Since electrical and optical domains merge in PICs, optical and electrical equipment is needed. In the long run, testing should be as automated as possible, meaning that wafer level testing should provide known good dies, reducing the fraction of dies that need to be tested at the package level. However, standard wafer probe stations are mainly intended for electrical testing, so the main challenge is to customize the probe station so that it is equipped to carry out complete (optical and electrical) testing. After dicing, a pick-up element with accompanying alignment metrology is necessary to release and properly place dies for testing on a thermally controlled stage.

CRITICAL (INFRASTRUCTURE) ISSUES

In general, the ambition in manufacturing is to measure as little as is necessary to gain the relevant information on product quality. However, to reduce the **assembly related** costs it is essential to closely monitor the complete fabrication process of the photonic integrated circuits (PIC) or even of the final device. While this may appear to be a very expensive procedure, test and selection after fabrication and assembly is even more expensive. A critical point here is to select the good dies at a very early stage (i.e. the wafer stage) in the manufacturing chain. This is referred to be as known-good-dies.

Beginning with wafer level production, each cleanroom step needs to be measured and validated. Since the silicon photonics manufacturing utilizes CMOS processes, it can benefit from such well-established characterization methods as ellipsometry, atomic-force microscopy (AFM), scanning-electron microscopy (SEM), white light surface profilometry and optical microscopy for layer thickness, critical dimension (CD) and line edge roughness measurements. These methods are well known and well established throughout the industry and, when used appropriately, can guarantee high throughput and high yield. For photonic integration technologies on other substrates and using other material systems compatibility with CMOS optimized tooling is limited, hence transfer of those test and characterization methods may require additional R&D efforts for adoption to such technology processes. In addition, the electrical tests of the integrated circuits are quite well established. Automated test equipment, test heads including specially adapted probe cards of different designs in combination with fully automated wafer probers contribute as well to a high throughput for the electrical measurements in manufacturing chain of integrated circuits (ICs). An exception to this is the need for electronic probes for very high bandwidth detectors, since it is not yet standard practice to automatically test electronic circuits at speeds higher than 40 GHz.

The equipment infrastructure for photonic measurements is not as mature as that for electrical test equipment. One major challenge for the coming years will be to assure availability of high volume and high throughput die & wafer level (WL) measurement equipment for photonic integrated circuits and electronic-photonic integrated circuits, so called EPICs. A logical step would be to extend the electronic test equipment to enable photonic measurements using a similar physical architecture. For wafer level measurements, this would correspond to optical solutions within the:

- Wafer prober / wafer handler
- Probe Card
- Automated Test Equipment (Test head or test matrix, measurement instruments)

The wafer prober and wafer handler need to be similar in structure. They handle the wafers, do the x,y,z and theta alignment and step through the devices on the wafer. A feedback from the automated test equipment is beneficial but all current probers are capable of handling such input. However, the prober needs to be optimized for the particular optical input/output ports to be probed. For example, an edge input/output requires an optical fiber probe with a turning mirror, and must be aligned both in angle and position (typically better than 1 µm) to accomplish the coupling. A grating coupler has more relaxed positional tolerance but requires precise angular control. In both cases, the mechanical requirements are more stringent than is required to probe electronic test pads. For very high speed applications, the electrical bandwidth of the probe card may need to exceed 40 GHz. When probing detectors directly, it is then helpful to include a transimpedance amplifier in the probe head.

There are currently several suppliers of automated test equipment who provide tools such as high-speed optical power meters or optical network analyzers that allow engineers to develop a measurement setup very similar to the IC test setups.

The real challenge is to feed and read out the optical and electrical signals together to and from the device under test. In case of pure electrical probe cards, the electrical contact needles (e.g. cantilever, vertical or MEMS needles) provide physical contact to the DUT bond pads. In case of standard IC probers, the alignment tolerances of several micrometers between electrical interface (needles) and device under test are quite moderate.

The optical interface will be realized by a grating coupler on the DUT side and a waveguide of some kind, e.g. an optical fiber, on the prober side. The lateral tolerances for such an optical interface are much tighter and lie in the sub-micrometer range. This gap between the two tolerance ranges will make it difficult to extent the electronic measurement equipment to the photonic measurements or even ensure a compatibility of common IC-Wafer level test equipment and procedures.

It is critical to correlate the physical measurements to both the specific functional measurements and the overall behavior of the photonic integrated circuit.

Some physical measurements (for example, loss measurements, spectral bandwidth, polarization dependence) are very straightforward. Others present a more significant challenge; for example, a suitable measurement of the effective index and group index of the waveguide mode and accurate measurements of the modal profile near couplers are critical measurements that are not yet standardized.

In future, calibration facilities will be needed to provide calibration targets which can be traced back to a standard. For instance, test PICs calibrated for known component loss, waveguide loss, and dispersion could be made available to equipment manufacturers, foundries and packaging facilities. This is especially important when new materials are introduced; in such cases both the performance from a materials standpoint, as well as a device performance standpoint will be vital. Calibration facilities could be e.g. NIST (USA), PTB (Germany) or NPL (Great Britain).

TECHNOLOGY NEEDS (RELATED TO MILESTONES)

This chapter focusses on the technological needs regarding testing tools, methods, measurement time, capacity, speed, and accuracy. For an efficient workflow between the different production partners (e.g. design houses, wafer processing fab, backend and packaging groups and customer) standardized measurement techniques with defined measurement data transfer are a stringent requirement. These topics will be addressed in the following sections.

PRIORITIZED RESEARCH NEEDS

Prioritized research needs that require results in less than five years include the following:
Ability to test photonic properties of wafers during fab to ensure that wafers are good.

Processing ever-faster (100Gbps+) data streams. Test time is often determined and limited by memory I/O data rates so increasing these will remove a barrier to lower cost. Developing test equipment with more capability than the devices to be tested is a continually moving target!

There will be a need for test platforms that are compatible with the test needs of different applications. It will be therefore necessary to separate, where possible, baseline testing needs from application-specific functional tests. Some examples of baseline testing are: component and connection loss measurements; parametric measurements (e.g. signal vs. temperature, wavelength, polarization); wavelength and wavelength-spectrum measurements; detector efficiency, etc. Some examples of application specific functional tests are: Bit-Error-Rate-Test (BERT); modulation depth and modulation bandwidth; calibration of phase shifters, etc.

PRIORITIZED DEVELOPMENT & IMPLEMENTATION NEEDS

Eventually, the ability to support 500 Tbps/fiber data transfer rates will be needed. An important issue is the nature of the data stream; how much parallelism, what modulation format, etc.

DESIGN

Standardization of test metrics and qualification

For any desired photonic-IC-based product, there can be numerous different implementations that will meet the same required result. Some of the options to consider are:

1. material system (InP, Si, GaAs, polymer, Triplex, glass),
2. integration scheme (monolithic, hybrid, heterogeneous, free-space component based),
3. packaging (non-hermetic, hermetic, housing material),
4. optical alignment (fibers, fiber arrays, lenses, grating couplers, vertical mirrors).

Therefore, standardized testing and qualification is an indispensable step towards reliable photonic-IC-based products independent of the particular implementation that was employed.

The measurement- and qualification rules of the electronic ICs are not sufficient to qualify photonic ICs, since these do not consider the optical parameters. Generally, photonic signals are more susceptible to environmental conditions/changes than electronic signals. In addition, sub micrometer alignment accuracy of fibers/lenses to photonic IC requires the use of mechanical/chemical-based fixtures with different materials with different properties, which makes that the performance not only depends on the photonic IC itself, but also is heavily dependent on the type of packaging. As a result, new standardized testing methodologies and qualification parameters need to be devised that apply to all technologies, all types of packages, and all relevant environmental conditions.

In order to monitor the full supply chain of the PIC product, testing has to occur on the following multiple stages:

1. during PIC Design: design of all the structures for the testing purposes mentioned below, add a standardized test device to monitor the performance of the PIC along the optical path (such as using a directional coupler to tap a small portion of the light and couple that to a sensitive photodetector or a grating coupler or vertical mirror to see the spectral characteristics)
2. on Wafer Level: measurement of process-related parameters that are relevant to the performance of the devices on the PICs (waveguide width, etch depths, contact- and series resistances, grating depths, etc.), wafer-release measurements at the end of the fabrication (preferably, but not necessarily, fully electrical using the light sources and the detector devices on the wafer) to determine whether the devices meet the targeted criteria, electrical- and optical on-wafer measurements using grating-coupler- or vertical-mirror structures for determining/estimating of the yield of the wafer (pulsed measurements with a standardized pulse width)
3. on Bar Level: testing of the coating performance, testing of the far-field pattern of the output waveguides, PIC testing using multiprobes/fiber arrays to select the known-good-dies for packaging afterwards
4. on Die Level: selection of the known-good-dies that were not damaged by the singulation process
5. on Packaged PICs: full testing of the PIC performance on the final package with the proper heatsink, burn-in of the PICs, final selection of the PICs that meet the targeted specs
6. during qualification: standardized qualification tests (such as temperature, humidity, shock, vibrations, etc.) for the environmental conditions relevant to the location where the PIC will be deployed

An important element of the standardized testing is the exchange of information between the various parties, and therefore, all data collected along the production line: design – wafer processing – backend – packaging – system tests should be stored in a standard data file format to enable an easy and simple exchange of the data between the partners. A centralized data base for all the data is needed to allow for a traceability of the full production processes.

Cloud sharing of the data could be a possibility to share the data, provided that IP issues and safety regulation allow this.
The implementation of an industry standard regarding the data format is needed.

Depending on the material system used standardized test protocols should be implemented that define the testing conditions such as e.g. temperature, moisture, surrounding atmosphere, maximum operation conditions, etc. In order to achieve a comparableness of measurements from different companies. This includes also a definition of the measurement equipment including the required minimum specifications. In some cases, e.g. optical linewidth measurement, also the measurement principle, e.g. homodyne or heterodyne approach, have to be defined.

Special tests structures have to be defined and processed with all wafers in particular for multiple-project wafer runs to allow for the tracking of the processing quality. All measurements should be defined in a way that the results will be operator independent. The measurement itself should be as simple as possible with a strong analytical significance. The choice regarding the most suitable measurement method should be driven by cost-awareness and economic considerations. Furthermore, the measurements should allow a correlation between measurements at an early stage and a later stage in the production line.

All measurement/tests in principle should allow for an upscaling for volume and mass production.

Tools and methods

As mentioned above in most cases special test structures that allow to track and check the processing and device quality have to be defined and processed.

A generic four step method should be implemented leading to a steady improve of the processing quality and the device yield:

Step 1 Investigation of many variations:
The processed test structures will be used to measure and evaluate the critical dimensions, such as

1. variations of processes (width, thickness, sidewall angle, etching depth, alignment, etc.)
2. variations of optical and electrical properties
3. variations of module properties

Step 2 Simulation using obtained variations:
If Step 1 is carried out at a large number of processed wafers (>100) designers can take the collected data and simulate the variations of some of the optical and electrical properties using the known variations of the processes (similar to Joint Test Action JTA in the electronic world). Thus a correlation between design, process variations and measurement results can be found. This can lead to a redesign of the respective components to increase the functional yield of the devices taking the processing variations into account.

Step 3 Decide on necessary and sufficient testing structures
When required the designer can develop novel and improved test structures to be implemented on the wafers.

Step 4 Storage of test data, reduction of testing components
By repeating Step 1…3 in combination with a careful analysis of the stored data the number of testing devices to be measured and tracked can be reduced and in parallel the yield of the functional devices will increase. A close collaboration between the designers and the Fab engineers is required here.

Examples for suitable tools for in-line testing are listed below:

1. critical dimension SEM (line width, hole diameter, line edge roughness)
2. atomic force microscope (line width, etching depth)
3. film metrology equipment (film thickness)

4. step measurement setup (etching depth)
   - ellipsometer (absorption, refractive index, thickness)
   - mass spectrometer in etching systems
5. optical material detection systems in etching systems
6. opto-electrical wafer probe setups for on wafer characterization
7. optical measurement equipment for optical loss measurements
8. photoluminescence measurement equipment
9. x-ray system for strain measurements

Ideally, the goal for the measurement method should be to extract the scattering and transfer charactieristics (S-parameters) of all the devices on the chip. These allow to create calibrated, compact models representing indicvidiual on-chip functions (building blocks) and enable more accurate simulations of the performance of the full functional chip. The extraction of the S-parameters can only be done by measurement methods such as the optical coherence reflectometry (OCR). The InP chips should be able to integrate an OCR on the chip, but for the Si- and the Triplex technology it is going to be more difficult.

High throughput testing (sub second per chip)

For volume production of photonic chips fully **automated testing** (e.g. waveguide defect testing, waveguide loss testing, laser performance testing, building block testing, actuator testing, etc.) is required.

Automatic testing comprises on the one hand inline automated testing at wafer level, such as e.g. critical dimension SEM, ellipsometric layer thickness measurement or step height measurements. On the other off-line automatic testing at wafer, bar/die and module levels are included. Examples for such offline measurements are frequency response measurements, output power measurements, responsivity measurements, etc.

High throughput, automatic measurements require standardized measurement procedures in combination with a standardized data format to enable an efficient data exchange between designers, engineers and customers. For large volumes (mass production) simple automated measurements will not be sufficient. In this case a **massive parallel testing** will be required in order to cope with the large number of devices to be tested and to bring the costs for testing down.

Only with massive parallel testing the average testing time per chip can be reduced, which is the main cost driver here. However analog to the electronic world massive parallel testing will only be applied if the number of chips to be tested has a significant magnitude. Typically, prior to those massive parallel test equipment the test procedures will be developed and tested with a single device test procedure. To enable massive parallel testing suitable standardized layouts, tests and package templates have to be developed. Also sacrifice chip area has to be defined if needed. In most cases these areas will be located near the dicing line and at the wafer edges. Most of these measurements will be carried out on wafer level, however part of the measurements will have to be carried still out on bar/die level. This is explained in more detail in the following two sections.

WORKFORCE DEVELOPMENT

It is well known that testing requires not only appropriate facilities and dedicated measurement equipment, but also experienced personnel. Broadly speaking, PIC testing can be performed by three different agents: foundries, test houses, and finally end users, with each being carried out at different stages of the development process.

The design and test development of regular electrical ICs needs a highly technically skilled workforce. PICs need a similar skillset, with the addition of engineers who have deep understanding of optical parameters, optical performance in photonic IC and module design and integration, as well as the manufacturing processes to achieve a working photonic module and manufacturing processes to achieve high yields. Ph-D level, engineers and technicians who have an understanding of technology, optical and electrical design and characterization and

packaging technologies and the leverage into high volume manufacturing are desired. The constant communication and interaction of the engineers who have these skills is needed to achieve an optimal design that is highly testable in the bring-up lab and on ATE. During the new product introduction phase teams of these engineers need to be highly engaged in debug and any redesign required to help achieve manufacturing yield goals. Manufacturing test programs for the optical and electrical parts are highly customized for the application and are ideally done by test engineers who can work alongside the design team during the test development phase. Once done, the test programs can be handed to the high-volume manufacturing test houses, with a clear technical hand-off to make sure the testing is run correctly. Ideally the test house has equivalently skilled engineers who can take over the production testing and be the first in line resource of troubleshooting when any production test issues arise.

Testing is essentially manufacturing activity, and thus it requires education and training in a series of disciplines and skills. Table 3. Academic Education Requirements and Table 4. Training Requirements provide some guidance on these needs.

Table 3. Academic Education Requirements

Knowledge Required	**Content**
AC and DC electricity & electronics	Voltage, current, frequency, power, electronics, transformers, capacitors, inductors, transistors, ions, conductors, semiconductors, non-conductors, electrical to optical and optical to electronic conversion.
Basics of Optics	Ray tracing, lenses, mirrors, prisms, wavelength, phase, polarization, intensity, beam divergence, beam focus, optical modes, E and H fields as related to the Poynting Vector, light in fibers, both single and multimode, etc.
Characteristics of Signals	Power, transmitting information, signal to noise ratio, modulation methods including OOK, orthogonal signals, multiplexing, demultiplexing, Shannon Limit, etc.
Basics of Statistics	Gathering data, maintaining integrity, managing data bases, standard deviation, mean, median, Parato charts, statistical process control, control limits, Cp, Cpk, etc.
Measurements	Basics of mechanical, electrical, optical metrology. Repeatability, gage studies, etc.
Financial basics	Basic business financial concepts; revenue, costs, elements of cost, product cost elements, overhead, cash, AR, AP, depreciation, equity, etc. "The $ in must be greater than the $ out". "We make investments in order to make more money back utilizing the result of the investment," etc.
Design for Test	Understand and implement desing for test (DfT) concepts. Transfer product and application requirements, boundaries of manufacturing processes into test protocols. Understand implcations resulting from such and account for at the design phase of a PIC product. Master design and simulation practices using software tools and aid the product design team

Table 4. Training Requirements	
Skill Require	**Areas of Training***
Personal Behavior	Show up on time. Be prepared to perform your job.
Safety	Rules, behavior, precautions, etc., related to safety for machinery, chemicals, slips and falls, people related, spills, MSDSs, PPE, “see something, say something” rule.
Quality	Follow the rules. Ensure procedures are followed. Go beyond the formal requirements and propose improvements. Follow the Japanese “5S” rules. Follow “Deming’s 14 Rules for Management”. Use statistics to improve yield and minimize variation.
Cost	Why cost is important, sources of cost, minimizing cost, proposing cost reductions, minimizing waste, maximizing reuse and recycling.
Equipment operation	Safe operation, instrument setup, calibration, standard operations, maintaining records, impact of each process on cost, use of the operating manual, machine maintenance.
Metrology	Use of callipers, electronic and optical measurement methods, storage of data and analysis, ensuring accuracy.
Interpreting Instructions	Read what it says, ask question, make sure you understand, do not “assume”, eliminate and resolve ambiguities,
Completing Jobs On Time	Ensure you understand what is required; ensure all of the instructions, materials equipment and other resources are available. Start as soon as possible. Look for potential barriers ahead and ensue they are eliminated. Be prepared to revise your approach. Ask for help. When you make a mistake, admit it, learn from it, ensure you do not make it again. Do not hide your errors.
*While training is often highly specific to each job, basics apply to all jobs.	

GAPS AND SHOWSTOPPERS

STANDARIZATION

Standardized testing metrics and procedures are essential for developing PIC markets further. Some specific killer applications (interconnects, automotives, sensors, etc.) are needed to accelerate the standardization. Necessary test items depend on a particular application, and a specific application makes them clear. A promising big market provides a powerful incentive for PIC companies such as PIC device companies, PIC foundries, PIC testing equipment companies.

Necessary test items should be standardized across full PIC value chain. Testing designs and procedures are then standardized. The design tools for testing should be implemented in EPDA and PDK. Testing should be accuracy and fast. On-chip self-diagnostics like that of EICs will be needed in the future.

PIC device engineers have to clarify testing equipment specifications (electrical and optical probes, functionalities, accuracy, speed, etc.). They should collaborate closely with PIC testing equipment engineers.

The standardization seems a difficult challenge in this field because it needs many people’s efforts and some sufficiently attractive markets. If this challenge is achieved, we will be able to develop various kinds of PIC products with a minimum of effort.

PLATFORM AGNOSTIC TESTING

The basic testing setup is common in a variety of PIC technologies (SiPh, InP, GaAs, SiN, polymer, etc.). Technology agnostic testing is very important. The standardized testing equipment should be used for a variety of PIC testing with minor modifications. Various PIC companies should corporate with each other across technical boundaries. The PIC devices are tested at a variety of sample shapes (wafer, bar and die). Sample-shape agnostic testing is also very important.

AUTOMATION

Fully automated PIC testing equipment are essential for developing PIC markets further. Mature EIC industry test practices should be emulated, and original PIC industry test practices should be developed. Various types of fully automated transceiver testing (OOK, PAM4, QPSK, 16-64QAM, etc.) will be needed.

HIGH SPEED (RF BANDWIDTH) TESTING

PIC testing equipment have to measure both low-speed and high-speed properties. Fully automated high-speed test (> 10-100 Gbps) at wafer level are not easy. Probe contact becomes critical. We have to investigate which of the commonly used probe technologies for high-speed electrical wafer level testing are compatible with optical testing (e.g. some probe cards will make it difficult to probe optically).

OPTICAL TESTING FOR MANUFACTURE

Contactless and non-destructive inline optical testing equipment with no particle pollution, which is acceptable for a PIC fab, will be needed. The inline optical testing can improve a product yield.

USER SUPPORT

User-friendly GUIs and a variety of testing scripts are needed. PIC tests are generally difficult because electrical and photonic knowledges are needed. So, helpful training manuals and courses are necessary.

ANALYSIS OF TESTING RESULTS

We have to research relation between testing results at each level and product performances. A PIC accept-reject methodology should be established for each product. For example, one faulty sub-system does not necessarily disqualify functionality of the full circuit. In addition, statistics and analysis of testing data should effectively be transferred across the PIC value chain.

COST

Fully automated optical and electrical testing equipment will be very expensive. We should share expensive testing tools based on standardization and platform agnostic testing. Testing time (including setup, calibration, wafer load and unload etc.) should be enough short because time is money. But testing should be enough accuracy.

We have to make the best use of testing results to achieve a good product yield and a high product performance. The testing results should be also used to revise a product design and develop new products with much higher performance.

HIGHER PIC TECHNOLOGIES

Some specific applications help to solve the above problems. Higher PIC technologies are necessary to realize such applications. For example, low loss propagation, low power consumption and high speed optical modulation, photo detection, and amplification, high temperature stability, high r_{33} materials etc., which translate into high performance, will be expected in SiPh, InP, GaAs, SiN, polymer, etc.

- The 50 GHz barrier resulting from conventional CMOS capability forcing parallel solutions rather than higher baud rates.
- Low speed of suitable assembly, test and other process equipment resulting in high costs.
- Inability to overcome the cost driving, rate limiting step/bottle neck of manufacturing/testing such as the number of assembly steps or length of time to perform test, especially BER testing. **"Time is money"**
- Limits resulting from adopting existing equipment, materials and methods to optical test as more specific equipment is not available. Currently the demand for such specialized equipment is not sufficient to incentivize equipment manufactures to make it available due to high non-recurring engineering (NRE) costs and low return on investement.
- Designing for Manufacturing and test:
  - Maximizing output to reduce cost
  - Studying designs to trade off accuracy and speed
- Inability to utilize materials or processes due to environmental related constraints (RoHS, REACH, WEEE, etc. TBD)

RECOMMENDATIONS ON POTENTIAL ALTERNATIVE TECHNOLOGIES

0. Silicon waveguides to 1D/2D photonic crystal waveguides or plasmonic waveguides. Some devices become much smaller (-> high density photonic integrated circuits).

1. Combinations of active and passive polymers for alternative Silicon (and other) PIC designs and automated test, calibration and verification procedures

2. Utilize laser processing to make optical waveguides in-situ to effective optical connections and optical structures.

3. Utilization of plasmons to minimize size and maximize functionality

Contributors

Tom Brown, University of Rochester - chair
Dave Armstrong, Advantest - chair
Sylwester Latkowski, Photonic Integration Technology Center, Eindhoven University of Technology - chair
Robert Pfahl, iNEMI
Graham Reed, University of Southampton
Dan Evans, Palomar Tech.
Richard Otte, Promex Industries Inc.
Bill Bottoms, 3MTS
Lionel Kimerling, MIT
Makoto Okano, AIST
Martin Möhrle, Fraunhofer HHI
Tobias Gnausch, Jenoptik
Michael Lebby, Lightwave Logic Inc.
Jeroen de Coster, IMEC
Chris Roeloffzen, LioniX International
John MacWilliams, Consultant
Willem Vos, University Twente
Chris Coleman, Keysight
Jan Mink, VTEC
Keren Bergman, Columbia University
Gordonn Liu, Huawei
Sam Salloum, Tektronix
Jan Peters Weem, Tektronix
Scottie Wyatt, Tektronix
Iñigo Artundo, VLC Photonics
Rocio Banos, VLC Photonics
Michael Garner, Stanford University
Robert Polster, Columbia University
Philip Schonfield, RIT
Ignazio Piancentini, Ficontec
Shangjian Zhang, UEST
Eugene Atwood, IBM
Zhihua Li, IME
Yi Zhang, Teradyne
Zoe Conroy, Cisco
Fen Guan, Global Foundries
Carl Buck, Aehr Test Systems
Tsuyoshi Horikawa, Photonics Electronics Technology Research Association (PETRA), Japan

We would like to thank all who contributed to the Test TWG, both in workshops, on-line conferences and with written comments.

Fair use disclaimer: this report contains images from different public sources and is a compilation of the opinion of many experts in the field for the advancement of photonics, the use of which has not always been explicitly authorized by the copyright owner. We are making such material available in our efforts to advance understanding of integrated photonics through the research conducted by the contributors of this report. We believe this constitutes a fair use of any such copyrighted material as provided for in section 107 of the US Copyright Law. In accordance with Title 17 U.S.C. Section 107, the material in this report is distributed without profit to those who have expressed a prior interest in receiving the included information for research and educational purposes.