# PHOTONIC DEVICE TESTING

## SECTION 1: OVERVIEW

For years, the microelectronics industry has continued to invest in electrical high-speed IO solutions. This caused broad deployment of optical components to continually shift out in time. With the rising challenges of electrical high-speed signal delivery and resulting higher power levels, a shift to optical techniques is quickly becoming the path of least resistance. Inherent in this direction shift, the industry needs to converge on an easily replicated, cost-effective photonic device test solution.

The present hope of the industry is that photonic device testing will follow the model refined over decades of use for silicon device testing. Two example flows are shown below. The top flow is typical for front-panel pluggable optical transceivers. The lower flow is more typical of chiplet-based, optical engine-based designs.

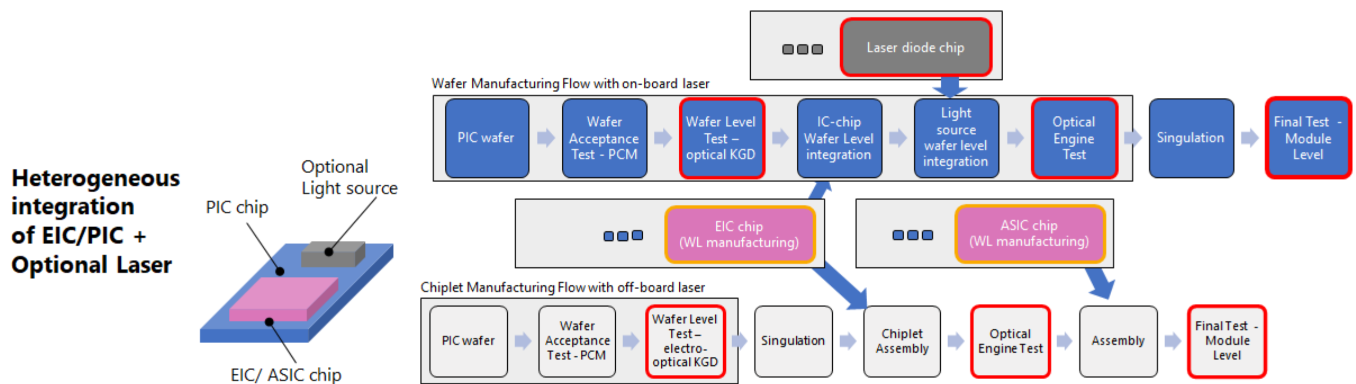


Figure 1: Two different manufacturing and test sequences.

A very important difference between the two flows in Figure 1 is the laser location. In the lower flow, the laser is kept off-board, similar to a power supply for the device. This simplifies the assembly and reduces the heat generated by the laser remote to the assembly. The upper flow adds the laser on top of the interposer as shown in the graphic.

Figure 2 shows the “purple brick wall” for data-center optical components. This graphic highlights the key test requirements as driven by the target device and the quality goals demanded by the next step in the manufacturing process.

Optical test methods will be needed in three different locations – each with their own focus and test-content:

1. Wafer Probe (PIC) Test – this will always be done at the wafer fabrication facility. Key questions remain regarding optical coupling methods and test content. These are discussed in the next section. One of the unusual challenges associated with this test insertion are the high-yields which are typical at this stage in the product lifecycle.

2. Chiplet Test (Optical Engine) - this will typically be performed where the multi-die assembly takes place, which is often at the sub-contract manufacturer. In order to assure a high module yield, it is critical that the optical engine test sequence target and achieve a known-good device, all the while doing this with interfaces which have not yet been solidified. This challenges the industry to achieve

new levels of alignment precision while keeping the costs and test times to a minimum.

3. System Level (module) test: final test will be done at the sub-contract manufacture in order to confirm the yield of the entire assembly. In addition, the end-user community will typically perform the final test step by sending large quantities of mission-mode test content through the device, while carefully watching for any and all errors which occur. Since test times can be very long, smart and careful selection of test content is key to minimizing the cost-of-test.

The true challenge for the industry is how to manage three test insertions in such a way that the test costs don't spin out of control. Some key factors which may help or hinder this cost equation are:

1. High cost of test consumables
2. High PIC wafer level yield today, which may fall with more complex devices
3. How to get the best cost-of-test when factoring in the various interface speeds

Figure 3 shows the "purple brick wall" for other types of optical devices (LIDAR & Sensors). With this year's update we are focused on testing data-center components. It is presumed that LIDAR and sensor testing will benefit from this discussion. In a future update, specific data on meeting the test needs of the LIDAR and Optical Sensor market segment should be explored.

The status of testing of photonic devices might best be summarized by stating that we have all the puzzle pieces we need to meet the need. Now our challenge is simply to assemble them in the most efficient fashion and start shipping products.

| | CY2022 | CY2023 | CY2024 | CY2025 | CY2026 | CY2027 | CY2028 | CY2029 | CY2030 |
|---|---|---|---|---|---|---|---|---|---|
| Modules/TxRx<br>Data rate density<br>Form factor | 400 Gbps<br>25 Tbps/1U<br>QSFP | 800 Gbps<br><br>QSFP/OBO/CPO | 100 Tbps/1U<br>Optical Engine | 1600 Gbps | 400 Tbps/1U<br>Optical Engine | | 1600 Tbps/IU<br>Optical Engine | 3200 Gbps | |
| Test Rate/Signaling during test | 64 Gbps/NRZ<br>56 GBd/PAM4 | | 128 Gbps/NRZ<br>64GBd/PAM4 | | 256 Gbps/NRZ<br>64GBd/PAM8 | | | | |
| WDM # of wavelength during test | CWDM | | 4λ | | 16λ | | 32λ | | 64λ |
| Test Solution Concept | Home Brew,<br>Rack & Stack | | ATE + Rack &<br>Stack | | @ATE Optical<br>Engine test | | @ATE At-speed<br>Optical Engine | | Multi-Site<br>optical DIT test |
| Optical Component Types to test | Test samples<br>for eval. | Switch, VOA<br>PD, SSC, Coupler | Modulator &<br>Receiver (32G) | WDM MUX &<br>DEMUX | | Modulator &<br>Receiver(128G) | | | |
| Laser source power during test<br>Laser Lambdas | 80mW DFB<br>(CWDM gird) | | 120mW<br>(CWDM gird) | 180mW<br>(CWDM gird) | | | | | |
| Optional functions<br>★ per pin resource<br>☆ shared resource | | ★TE⇔TM<br>converter<br>☆Spectrometer | ☆Tunable Laser<br>★Reflect test | | ★Polarization<br>controller | | | | |
| Device Interfaces | PIC = Grating<br>couplers &<br>PigTails | | Grating/Edge &<br>Proprietary<br>sockets | Grating/Edge &<br>Proprietary<br>sockets | Grating/Edge &<br>Standard<br>sockets | Waveguides in<br>interposers. | Wafer, Die test<br>solution @speed<br>(needed?) | | Free air<br>interconnects? |
| Optical impairments in loopback<br>path to do a good test | | Attenuation | | Dispersion<br>Polarization<br>control/adjust | | | | | |

*Figure 2: Purple Brick Wall for Testing of Data Center Components*

| | CY2022 | CY2023 | CY2024 | CY2025 | CY2026 | CY2027 | CY2028 | CY2029 | CY2030 |
|---|---|---|---|---|---|---|---|---|---|
| **Lidar (Platform/Package)**<br>TOF/FMCW | InP, SiN, Si<br>(Hybrid package) | | InP, SiN, Si<br>(Hybrid package)<br>DC + RF+ Fiber +Free Space | | InP, SiN, Si, Low-loss thin-film lithium niobate (TFLN) (Hybrid package)<br>DC + RF+ Fiber +Free Space | | | | |
| **Interrogator System (Platform/Package)**<br>Tunable Laser based/<br>Interferometer based/<br>Spectrometer based | InP, SiN, Si<br>(DC + multi-fiber I/O<br>(non-PM SMF) | | InP, SiN, Si<br>(Hybrid package)<br>DC +multi-fiber I/O (PM and non-PM SMF) | | InP, SiN, Si, Low-loss thin-film lithium niobate (TFLN)<br>(Hybrid package)<br>DC +RF + multi-fiber I/O (PM and non-PM SMF) | | | | |
| **Sensors (Platform/Package)**<br>Spectral Sensors<br>Medical/Environmental/chemical/gas sensing/industrial | | | Si, SiN, Ge<br>Hybrid package<br>Fiber +Free space Interface +DC | Si, SiN, Ge, InP chalcogenide<br>Hybrid package<br>Fiber +Free space interface +DC | Microfluidics packaging | | | | |
| **Wavelength Range**<br>Lidar/Interrogator/Sensor | C+L | | O+S+C+L+U | 3-5 um | 8-12 um | | | | |
| **Optical Components**<br>Lidar/Interrogator/Sensor | MZI, Spectrometer,<br>Phase modulators,<br>Amplitude modulators<br>Ring resonators,<br>Spectrometer, PDs | | Polarization controllers<br>Fast modulators<br>High resolution spectrometers | Low loss waveguides | | Optical isolators on a chip | | | |
| **Sources**<br>Lidar<br>Interrogator<br>Sensor | Tunable Lasers,<br>Broadband Sources,<br>Narrow LW Lasers<br>(40-80nm) | | Tunable Lasers,<br>Broadband Sources,<br>Narrow LW Lasers<br>(80-160nm) | Comb sources,<br>broad band sources,<br>multi laser on a chip | Tunable Lasers,<br>Broadband Sources, Narrow LW Lasers<br>(160-320nm) | | | | |
| **# of IO (optical/electrical)** | 8/16 | | 16/32 | | 32/200 | | | | |
| **Environmental testing** | 0 to 65 deg C | | -5 to 70 deg C | | -20 to 85 deg C | | | | |
| **Test parameters** | P, IL, λ, R, SMSR | Dispersion, FSR | Polarization, reflections,<br>Max beam distance | Refractive Index,<br>WDL | Temperature stability (IL and FSR vs T) | | | | |

*Figure 3: Purple Brick Wall for Testing of LIDAR and Optical Sensor Components*

Disclaimer: This is a work in progress with input from a broad range of companies. We have tried to generalize from everyone's input. Some deviation from this norm should be expected when delving into the details.

## SECTION 2: WAFER LEVEL PIC TESTING

Wafer-level test of photonic integrated circuits (PICs) has multifold interdependencies to other aspects of the device-under-test- DUT's manufacturing flow e.g., packaging techniques, optical coupling methods, on- or off-board light sources, test instrumentation and even business models of the respective companies.

The biggest and most fundamental challenge is still to combine the well-established and standardized electronic test flows with optical test procedures to generate a consistent methodology based on standards of the IC test ecosystem. The example of a typical data-center optical interconnect exemplifies the implications for wafer test. Figure 4 illustrates the block diagram of such a device. Here, the typical device-under-test (DUT) is a photonic chip with a number of electronic components like modulators and photodiodes, and pure optical components like filters and splitters, and polarization controllers. The driving electronics is implemented in an additional electric IC (EIC or ASIC) which is then heterogeneously integrated later with the PIC.

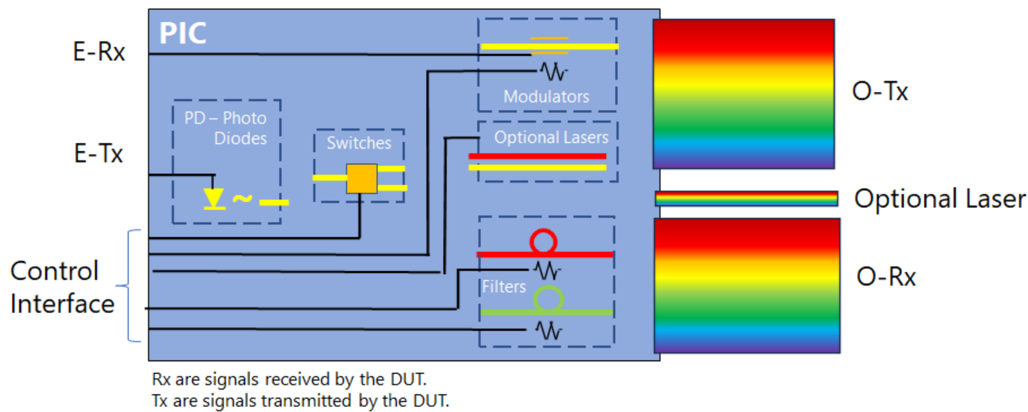


*Figure 1: Block diagram of a typical DUT for data-centers*

A typical layout of a data-center DUT in figure 5 illustrates the challenge of combining optical and electrical probes. The optical interface/probe needs to be close to the electrical contact. For a DUT layout with electrical pads in North-West-South configuration, the space constraints might be more relaxed than in a case where the coupling area is fully covered by electrical IOs. Introducing active alignment systems with 6-axis stages is challenging, although those systems are very suitable for characterization purposes, especially for edge coupling devices. The trend for electrical IO layouts is generally moving towards ball grid array (BGA) patterns and is driven by 2.5D and 3D packaging methods. For devices with a high number of solder bumps, vertical or advanced probe tips are required. That implies limited available space within the probe array and the tester. Here, a probe-card-like approach needs to be implemented.

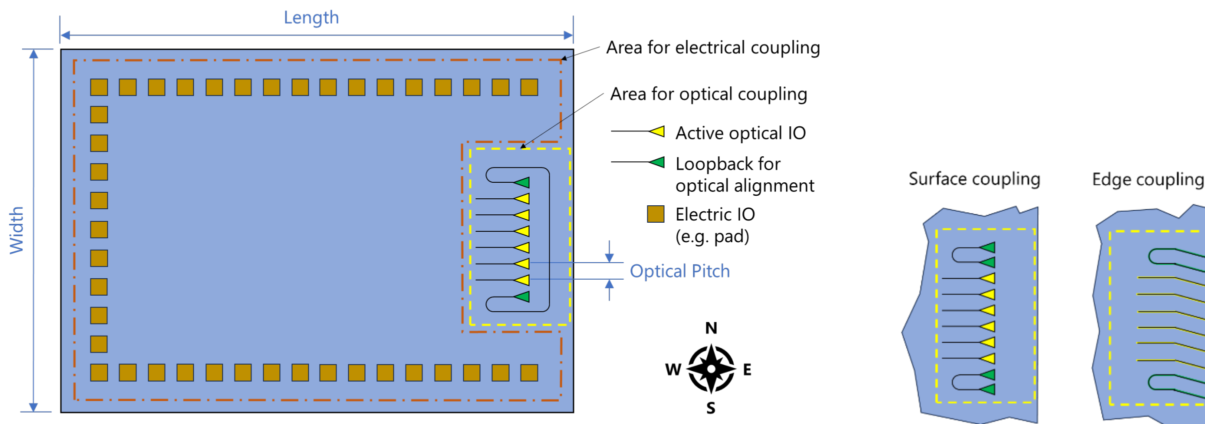


*Figure 2: Left, a typical generic layout of a data-center DUT with surface coupling. Right, other common layouts for optical PIC coupling including alignment features (surface and edge coupling).*

On- or off-board light sources pose another challenge, since light needs to be inserted to test. In the case of on-board light sources, the chip can be powered up electrically to emit the light. Chips with off-board or also heterogeneously integrated light sources, require an insertion from an external light source with a sufficiently low coupling loss.

In general, wafer tests of PICs will be less extensive than tests of electronic photonic integrated circuits (EPICs). There might also be additional wafer acceptance tests, for instance, on process control monitor (PCM) structures

required during manufacturing. However, monolithic integration of electronics and photonics into an EPIC is seen more often now.

Currently, PIC wafer-level test almost resembles a full characterization of all chip functionalities. In a ramp-up scenario, this needs to be adapted to a manufacturing test with a minimum of required tests and the use of common IC-test flows.

This incorporates dedicated Design for Tests (DFT)that could be implemented for specific PCM structures in case of low functional testing requirements of a stable manufacturing process. Well established processes might not even require any functional device testing but just PCM testing. Another way would be to implement surface coupling test structures even for edge coupling devices to adapt to common IC test procedures and flows. This can be done by e.g., sacrificial grating couplers in the dicing lane of the DUT.

Furthermore, the complexity of testing strategy can depend on the specific business model of the individual companies or entities. The extent of the tests could be greater if the wafers with photonic circuits were being sold as an optical engine to another party if they were being further integrated into a vertical manufacturing flow. Information from later integration steps won’t be available and thus needs to be extracted at the wafer test.

*Table 1a: Typical data-center PIC characteristics:*

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Chip dimensions | 2mm to 10’s mm | Wavelength | O and C-Band |
| # of low-speed electric IOs | couple of tens to low hundreds | # of wavelength | up to 4 |
| # of high-speed electric IOs | 32 (e.g. 2 or 4 per lane) | Optical coupling method | Surface coupling |
| Location of electric IOs | Pads often North-West-South configuration, Bumps/ pillar in a grid configuration (PDK) | # and location of optical IOs | one bar of 3-12 IOs |

Optical and electrical tests that are typically performed at the wafer-level are the following: Optical wavelength scan for Rx and TX, including optical amplitude modulation, extinction ratio, and side mode suppression ratio of the TX modulators. With a wavelength scan the electrical sensitivity of the RX photodiodes is measured. Sometimes a calibration of heaters in the TX modulator is done. Bit-error-rate measurements and build-in self-tests (BIST) at wafer-level apply only to EPIC devices.

The test instrumentation form factor moves from a lab rack & stack to more dedicated instruments in PXI format. This is to provide flexibility to easily tailor instrument setups to the different test needs. The installed base at OSAT companies is 100 - 1000's of classic wafer-level testers. These systems cannot support a variety of active alignment methods. For high volume manufacturing -HVM testing, a reduction in test time is essential for cost-reduction.

Another challenge is to handle data rate and the need to test at speed.  The use of ATE systems will be required for fast data acquisition, especially for EPIC devices and RF-testing, that could be either accomplished by optical loop-back methods or direct RF testing.

Eventually, optical instrumentation needs to be naturally incorporated into those test systems. As ATE systems have tight space restrictions that prohibit the use of active optical alignment strategies and tools for such systems, the use of an optical probe card approach will be necessary. Moving towards probe cards while electrical pin count increases drastically, as well as optical channels, will result in challenging probe card designs regarding volume, stiffness, thermal behavior, and handling. Solving this challenge will help to set up a reasonable test standardization.

Additionally, passive alignment methods are not suitable for all applications. Since there is no “winning” method yet, this will present the OSAT's with a major challenge to provide the foreseen volume ramp: stick to what they know/have or invest in new equipment that supports new methods.
Beyond these technical challenges, keeping the costs within an acceptable level will be vital. Automation and standardization of layouts, methods and instrumentation will be the key.

## SECTION 3: OPTICAL ENGINE TESTING

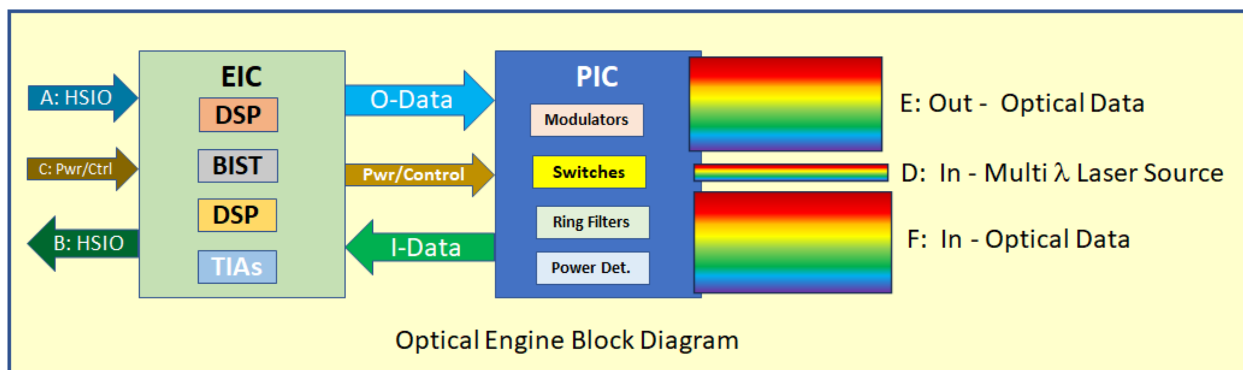


*Figure 6 shows a typical Optical Engine’s block diagram using an external laser.*

This two-chip assembly includes an Electrical IC (EIC) on the left which works in tandem with a Photonic IC (PIC) on the right. It will be manufactured using heterogeneous integration techniques (2.5D or 3D). The package construction does impact the overall product performance. A..F are the package level electrical & optical connections, and O-Data, Power/Control, I-Data are the IC-to-IC connections.

Looking at this drawing one sees that during a test we have a total of six possible access points (A~F) for the test. The diagram also highlights what must be the two goals for this optical engine test: 1) To confirm that the integrity of the three interfaces between the EIC and the PIC have survived the assembly process and are operational, and 2) To confirm that the two previously tested parts (PIC+EIC) are communicating appropriately.

Minimizing the number of interfaces contacted during a test will go a long way toward minimizing the cost of the test for this component. The two interfaces which must be contacted are “Pwr/Ctrl” (C) on the left side and the Laser Source (D) on the right side. In theory, all other interfaces can be somehow handled by design-for-test techniques such as loopback. Figure 7 below highlights the three basic types of loopback circuitry.

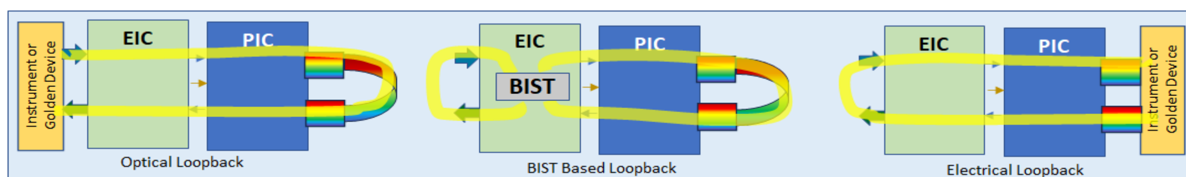

*Figure 7: Three basic types of loopback circuitry*

The Built-in-Self-Test (BIST) in the EIC, if present, will play a significant role in reducing the number of interfaces which need to be contacted. It can kick-off challenging data streams to the various high-speed interfaces (both electrical and optical) and if loopback is implemented on these interfaces, the BIST can then check validity of the return data stream. Bit-Error-Rate (BER) can also be calculated. A robust design will also enable both the electrical and optical loopback tests to be executed simultaneously thus minimizing test time.

If there is no BIST circuit, then a minimum of four interfaces must be contacted. This will include interfaces C and D as before and in addition one of the high-speed paths (Electrical A+B or Optical E+F) will need to be contacted and the remaining interface will need a loopback connection.

Since the laser input must be connected in any case, a natural solution would be to align and connect the entire fiber-array with the laser input(s) as well as optical connections to the various optical pins and outputs (E & F). Electrical loopback on ports A & B will allow testing of both the electrical Tx and Rx pins.

Use of the BIST based loopback approach will allow both high-speed interfaces to be tested simultaneously, including the driver and receiver circuitry. Use of the Optical and Electrical loopback schemes may require on-die loopback circuitry to avoid non-deterministic behavior in the external loopback circuit.

The various connection and data paths, including the three interfaces between the PIC and EIC can be tested for signal delivery. It's also important that any test which is implemented confirms the margins in the design. This requires that a high-quality test solution include the ability to accurately adjust and measure the following:

- Input laser wavelength*
- Input laser power level*
- Data Rates
- Supply voltage levels
- Modulator & filter tuning parameter
- Digital configuration cal value determination & fusing
- Optical Tx output level & polarization
- Optical Rx input sensitivity
- Optical engine temperature

* Should the optical engine have integrated lasers, their levels and wavelengths need to be measured.

Challenges to the optical engine test solution are many:

1. Device Handling: The handler must be capable of positioning the optical engine assembly (either interposer with chips attached or stacked chips) precisely under the probe card.

2. Fiber Alignment: The fiber and/or fiber-arrays need to be precisely aligned with the grating couplers (if vertical coupling is used) or waveguides (if edge coupling is used). Repeatable & reproducible fiber interconnect alignment is vital. The mechanical tolerances for package level optical connections are < 0.5uM and a radial accuracy better than 8°. Three different methods are being pursued to achieve this:
    a. Active alignment with a precision manipulator which uses feedback from the signals to minimize the coupling loss of the optical fibers.
    b. Passive alignment with an optical "funnel" which allows signal delivery with a little attenuation while using a traditional probe and/or handler with coarser alignment accuracy.
    c. A mission-mode optical connector if they are already installed on the optical engine. In this case the requirement for optical alignment becomes one to simply insert the connector for the test.

As the optical port counts scale, the challenges to achieve solid alignment on many fibers will grow significantly.

3. Temperature Control: Thermo-management of the optical engine is critical. While it is expected that the control logic will appropriately compensate for environmental temperature extremes, tests are needed to confirm that this logic is functioning correctly. Performing these tests will require the ability to program different calibrated temperature points during test execution.

4. Diagnostics and Calibration: Similar to standard automatic test solutions in production today, all signals, including the optical I/O need to have robust diagnostic and calibration procedures. This includes Diagnostics & Calibration for the test fixture and the package interconnect.

5. Probe Card Reliability: Like probe cards today, the optical test interface needs frequent cleaning and alignment. Contamination control of particulates is a particularly large concern when you're dealing with a fiber core with dimensions of only a handful of microns.

6. Optical inspection of the component itself before and after the test is also critical. Being able to inspect the waveguides and connect defects on that layer with testing data is crucial to get the process loop closed or at mature level. PICs+EIC's can also be very fragile. They can crack and cleave in non-intuitive ways depending on the underlying physical optical structures.

7. Firmware/Software: The EIC may well have a microprocessor and associated memory integrated in it. Confirming that the latest control software and firmware work with the device under test, may be required.

8. BER and eye-opening are certainly key parameters to confirm a Known-Good-Optical-Engine at time-zero and at end-of-life. Other tests will likely need to be added depending on each company's experience and focus.

9. Instruments required to do these optical tests include: Optical-BERTs, Tunable-Lasers, Switches, Power meters, Lightwave Component Analyzers, and Vector Network Analyzers. Each of these instruments may or may not exist for the desired wavelength, bandwidth, and performance level.

10. EIC & OIC requires electrical and optical test equipment integration. The use of rack & stack instruments increases the overall test cell size.

    A hard realization of optical testing is that the cost-of-testing these components will often be higher than similar sized silicon devices.

While all the pieces of an optical engine test solution exist today with various levels of performance and completion, the real challenge for the test engineer is to pinpoint what test content (with what margins) and with which instruments must be done at this test insertion in order to get a "Known-Good-Optical-Engine". Defining the Design For Test -DFT and analyzing the entire test flow up-front is critical to controlling costs and achieving a high-yielding product in the end. Getting the engine to a known-good state is critical for the yield of

the next level of assembly (the module). If the fault-coverage is deficient, a large multi-die assembly with multiple optical engines mounted on it will quickly show catastrophic yield losses.

## SECTION 4: OPTICAL MODULE TESTING

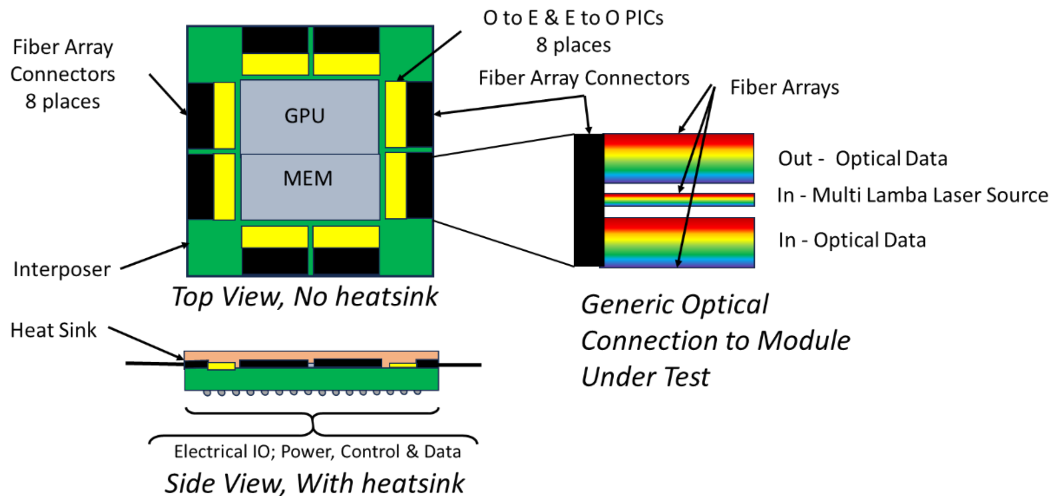


*Figure 8: Schematic of an optical module to be tested*

**Module Test**

The image in Figure 7 of a generic optical module to be tested has the typical characteristics, features and parts found in a server module. Laser sources are usually in a sub assembly module that is off-module due to their high-power dissipation and resulting need for heat sinking and temperature control. Laser light is taken to the module where modulators on the PICs impress data on light and send it off-module through fibers or arrays.

High speed data is usually brought into and taken from the module in fiber arrays of 12 to 64 fibers. The fiber connections to the module are most commonly through connectors as shown above but sometimes as pigtails, or short pigtails with connectors. Fibers or fiber arrays bring in high-speed data from light that is converted to electrical signals through the O to E PIC close to the GPU or memory or ASIC. Likewise high-speed output data is impressed on light through a PIC that has an E to O modulator.

MP and MTP connectors typically introduce 0.5 to 1.0 dB of loss, so their use is typically minimized.

Power, control signals and some data are brought to modules through electrical connections on the interposer or substrate as it is often called. Electrical IO is typically through solder balls (0.5 mm pitch) or, in high density devices, copper pillars (50-to-129-micron pitch).

During module test, the test station provides suitable light sources, electrical power, control signals, data to “test” the module functions and possibly some heat sinking or other method to control or vary the module temperature.

Module test follows die and wafer test but proceeds "Final test." A module is usually a sub-assembly but is sometimes a final assembly. A module may have several levels of sub-assemblies with more parts added at each level as the final product develops.

Modules are tested to ensure their characteristics meet requirements. The objective, of course, is to ensure that defective parts are removed from the assembly process as early as possible. In addition, defective parts are evaluated to determine the cause of failure and that information is used to improve the earlier processes and ensure that a higher percentage of devices meet requirements.

Modules to be tested can be simple, like a laser mounted on a substrate with a connector or it can be a highly complex device with multiple lasers, with bandpass filters, isolators, etc., multiple electrical controls, power and data ports and thermal "ports".

Testing requires handling the modules- meaning putting them into a test fixture, removing them after test and placing them in a container to move them to the next process. While the module is in the fixture, measurements are made, the data are characterized, processed in some manner, possibly recorded and then used, usually to determine whether the device meets the requirements.

BIST (built-in self-test) is incorporated whenever possible and is effective for checking electronic connections and functions.

Optical testing may require varying light intensity, modulation rates, polarization, wavelength, voltage level, etc. to ensure the SNR (signal-to-noise ratio) and BER (bit error rate) are acceptable within the allowed variation of the inputs.

Module test results are usually analyzed and the data "fed back" to earlier module assembly processes to ensure that devices not only meet spec but that the earlier process is monitored and modified to minimize variation in subsequent modules using Statistical Process Control.

Test time for many optical modules is inherently fast, meaning less than a second, as most phenomena (light intensity, wavelength, polarization, modulation rate, etc.,) can be measured in an instant. Some measurements require changing something like the laser source wavelength, temperature (0 °C to +85° C for production or -10 °C to +125 °C for characterization for example), drive voltage, etc., and those can take more time due to the rate at which the input variable can be changed.

A main determinant of the total test time is the handling time; the time to put the device into a test fixture, make electrical, thermal and optical connections, then disconnect the device after test and put it in a carrier of some sort. Optical modules often require careful handling because they are fragile. They may be "awkward" to handle if they have one or more optical connectors, optical fibers, fiber arrays or cables attached to them. Optical modules are usually physically small, weighing a few ounces or less, and require minimal space during manufacture, storage and shipping. Total test time is important due to its cost; the longer the total test time, meaning handling as well as making measurements, the higher the cost. Test equipment for modules that are built in "high" volume will be configured and built to minimize the test time. Designing and building that equipment for a particular module may be expensive so the system designer must decide how much effort should be spent to save test time. The larger the number of modules to be tested, the greater the effort that can be put into equipment to minimize module handling and total test time of course.

Some type of handling equipment for common module configurations is available commercially. These equipment lines often have multiple accessories and configurations that can easily be adopted to test a variety of optical modules. A critical element of this equipment design is the fiber handling and/or fiber array docking solution to mate with the module. Not only must this solution provide a reliable low-loss connection to the module, but it also needs to effectively clean and calibrate the optical surfaces.

A long-term important trend impacting module test is that toward smaller devices. Optical devices as small as 1 millimeter in diameter and 15 mm long are in use and becoming more common. These require specialized fixtures and more detailed handling.

## SECTION 5: SUMMARY

The challenges regarding the electronic-photonic test process for integrated photonics described in Sections 1-4 underline the timely relevance and importance of these processes. In addition to its well-established role in telecommunications, integrated photonics is becoming an inevitable technology for data center applications. Photonic integrated circuits aid high bandwidth, and low energy optical interconnects for a wide range of distances, from the inter-data centers links to inter-CPU interconnects. To fully benefit from the advantages provided by photonic integrated circuits, such optical engines must be intimately integrated with microelectronics using heterogeneous integration technologies. The latter makes integrated photonics, a part of the microelectronics industry. Consequently, the economies of scale that apply to the integrated photonics supply chains change as well. These aspects shall be also considered for other application domains such as bio-sensing and LiDAR.

The data-center application was used as a practical case study in this chapter. Such an example provided a focus allowing to narrow down the scope of discussions while rendering more tangible conclusions. The electronic-photonic test processes were broken down into three categories corresponding to the production flow of a PIC-based module, namely wafer level test, optical engine test, and module level test. While respecting a wide range of relevant technologies, and combinations thereof that allow for the delivery of desired functionality, the technical working group did put a particular effort into generalizing as much as possible while staying focused on the target application, being an optical transmit-receive (TxRx) module for a datacenter.

The total test time, including the handling, probing, and measurement could be considered the most important quantifier for all three categories. The total test time can be related to the acceptable cost for a particular product, accounting for the overall volume, and market value of the product.

The overall contribution of the test processes to the total cost of the production of the telecommunications module is presented in the figure below (Fig. 9, after [1]). Although it is based on published historical data [2], feedback and information provided by the working group participants, and more recent publications of the same model [3,4] allow it to be considered valid for a generalized PIC-based module. For different applications, for which the complexity of the integrated systems, the economy of scales will vary, therefore one should use this generalized overview with caution for a particular case.

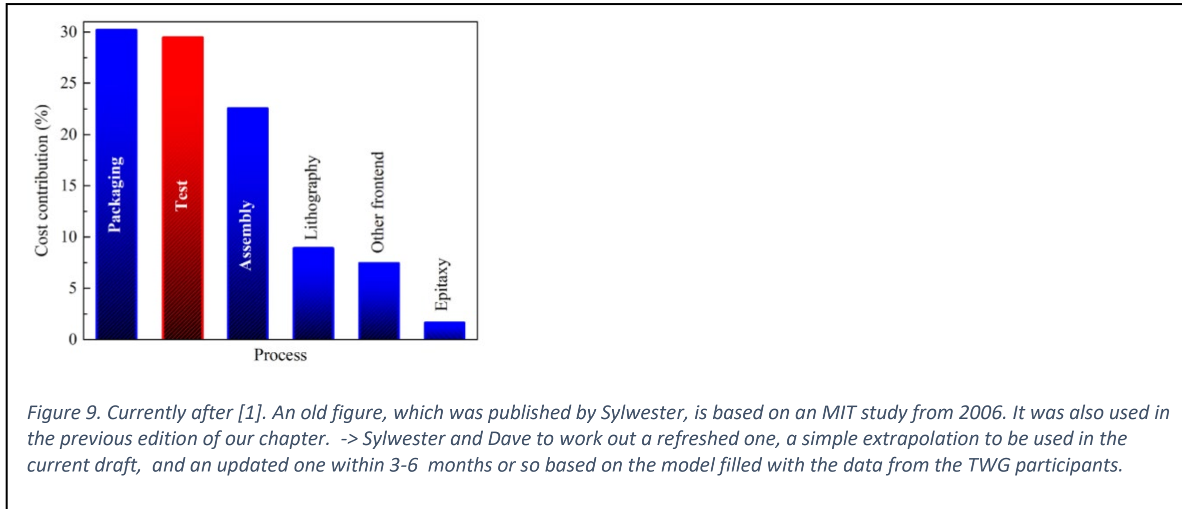


*Figure 9. Currently after [1]. An old figure, which was published by Sylwester, is based on an MIT study from 2006. It was also used in the previous edition of our chapter. -> Sylwester and Dave to work out a refreshed one, a simple extrapolation to be used in the current draft, and an updated one within 3-6 months or so based on the model filled with the data from the TWG participants.*

The cost of testing for electronic ICs in a mature process is around 2-3% [4] of the final product cost. The above indicates that the test in PIC's today is in a range of 25-30% of the final product cost. To fit the economies of scale following the microelectronics industry this must come down to an acceptable level. To reduce the cost the following should be considered: increased automation, increased standardization, revised design objectives, EDA environments enabling electronic-photonic co-design, heterogeneous (electronic-photonic) process design kits, and careful positioning of the RF test across the three categories of the product creation, as used in this chapter.

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