INP AND III-V COMPOUNDS

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Executive Summary

III-V semiconductor compounds form the core material systems of a wide range of discrete and eventually fully integrated photonic components (lasers & optical amplifiers, modulators, photodetectors, and passive-optical functions) and also high-performance electronic devices. A key feature of III-V compounds is that they exhibit a direct bandgap enabling efficient generation and amplification of light, as opposed to indirect bandgap semiconductors like silicon and germanium. Since the sixties of the previous century this has resulted in the development of a wide range of semiconductor laser types (CW, tunable, multi-wavelength, pulse, frequency-comb, single photon) for use as transmitters. Tuning the electron band gap of the material by alloying different III-V compounds enables the adjustment of the wavelength of the light to the required value within a fairly broad spectral NIR range. Materials based on GaAs (~ 850-1100 nm) and InP (~ 1200-1700 nm) are the most prominent systems in use, largely driven by fiber-optic communications. Thanks to this application field InP has achieved a superior role in integration of semiconductor lasers with a variety of structures enabling manipulation of the photons in photonic integrated circuits for a wide range of functionalities. More recently, GaSb-based diode lasers (1-8-3.0 µm) have attracted interest for light sources in sensing applications.

InP-based PICs have become firmly established in the market place, with suppliers and users shipping or deploying large numbers of complex PIC-enabled products today. A major advantage of InP-based PICs is their ability to integrate arrays of lasers and optical amplifiers in a single chip. Furthermore, integrated InP based modulators have demonstrated superior performance (driving voltage, efficiency). GaAs is mainly applied in VCSELs and VCSEL arrays. The present roadmap is restricted to InP technology, in future versions we intend to include more information on other III-V materials as well.

CURRENT STATUS

InP PICs, dominated by datacom and telecom applications, accounted for a 2B€ market in 2022, predicted to expand to >5B€ by 2027. A major portion of this market is served by vertically integrated companies, but generic foundries have been established which have the potential to broaden the application of PICs to module and systems manufacturers who cannot afford the large investments for a cleanroom fab and development of a qualified proprietary manufacturing process.

MAIN CHALLENGES

A challenge for InP is the lack of a large-scale manufacturing infrastructure. Although the existing infrastructure is adequate for today's market, the expected increase in growth will require major investments in scaling the infrastructure for manufacturing and testing to align with the expected market size. Scaling laws and scaling costs for InP monolithic integration are similar to those of silicon fabs. With the growing demand for high performance PICs with a high degree of integrated functionality and flexibility, it will be feasible to allocate the required investments to scale to high-volume manufacturing and hence reduce the costs for InP PICs.

As highest technical priority we see the adaption of today's manufacturing equipment, most of which is still operated manually, to fully automated operation. For increased operational efficiency and performance, it is important to move to larger wafer sizes: 4", which is already in use today, and 6". In the longer term, transfer from InP-substrates to silicon substrates is envisaged, while keeping the photonic layer in InP and its compounds. This will enable transitioning the processing of InP PICs to 8" and larger wafers but will demand processing equipment with adapted extended performance capabilities. Improved manufacturing capability in terms of precision and resolution will ultimately enlarge the component design space and advance building block performance.

Another priority is in PDK-development and automated testing. First PDKs (Process Design Kits), which offer designers a variety of building blocks without the need for a deep knowledge of semiconductor technology, were introduced for InP-technology more than a decade ago, but require further development: more and more accurate building blocks and better simulation capabilities. PDK development and automated testing for InP has a large synergy with silicon photonics.

The future needs with respect to the basic technology to allow for improved performance highly depends on the photonic building block under consideration. The ultimate performance achieved by each building block will be largely determined by the integration platform capability in close consideration to application specific requirements and the trade-offs of complexity and performance costs, manufacturability and yield.

NEEDS:

PURPLE BRICK WALLS

Needs < 5 years
- Fully automated process equipment (epitaxy/deposition, etching) with cassette loading
- Improved reproducibility of epitaxy/deposition and etching (<1%)
- Reduced defect density in epitaxial (re)growth
- 193 nm lithography tools for 4" wafers
- Lithography resist selectivity
- Improved passivation technology for non-hermetic packaging
- Test standardization and automation at building block and circuit level

Needs 5-10 years
- Move to larger wafers (6")
- Higher integration densities using membrane technologies

Needs > 10 years
- Move to InP processing on silicon substrates (8" and larger)

Development of InP PIC technology is expected to make steady progress over time on a number of metrics. Advancements in several aspects of the technology, however, are expected to require significant industrial research and development efforts. These *Purple Brick Walls,* shown in Figure 1, fall broadly into three categories: substrate technologies, device performance and fabrication process technologies.

There is a powerful economic incentive to transfer InP devices to silicon substrates in order to take advantage of more mature process technology and larger wafer sizes. Growth of high-quality III-V crystals on silicon substrates is a barrier that will require significant investment to overcome. In the medium term, transfer of prefabricated InP PICs to a silicon substrate for further processing can be considered, but this will also involve a large effort to develop new fabrication process for the hybridized wafer.

For device performance, significant efforts will be required to move device bandwidth to ~200 GHz and beyond. In the specific case of modulators, it currently appears to be difficult to improve efficiency to 1 V·mm while simultaneously keeping optical losses below 1 dB. It would, however, be possible to trade off these figures of merit for specific applications.

For InP laser sources, Auger recombination presents an important barrier to improved efficiency, and new materials will likely be required to sustain advancement. New materials will also likely be required to realize laser operation beyond 100 °C.

InP fabrication technology is expected to take advantage of equipment and techniques from mature silicon process nodes. The critically important lithography is impeded by a lack of available scanner equipment that can handle smaller 3" and 4" wafers. While such equipment has been demonstrated and could be built in principle, it will require nontrivial investments to realize. Additionally, InP substrates exhibits substantially looser limits on parameters such as flatness and thickness uniformity compared to silicon, presenting additional difficulties. Addressing this issue will be critical to advancement of the industry.

Epitaxial technology is expected to advance, but achieving layer composition better than 1% will be challenging for growth technology. On the other hand, improvements in layer doping are likely possible will require nontrivial improvem ents in the metrology equipment used to characterize grown layers.

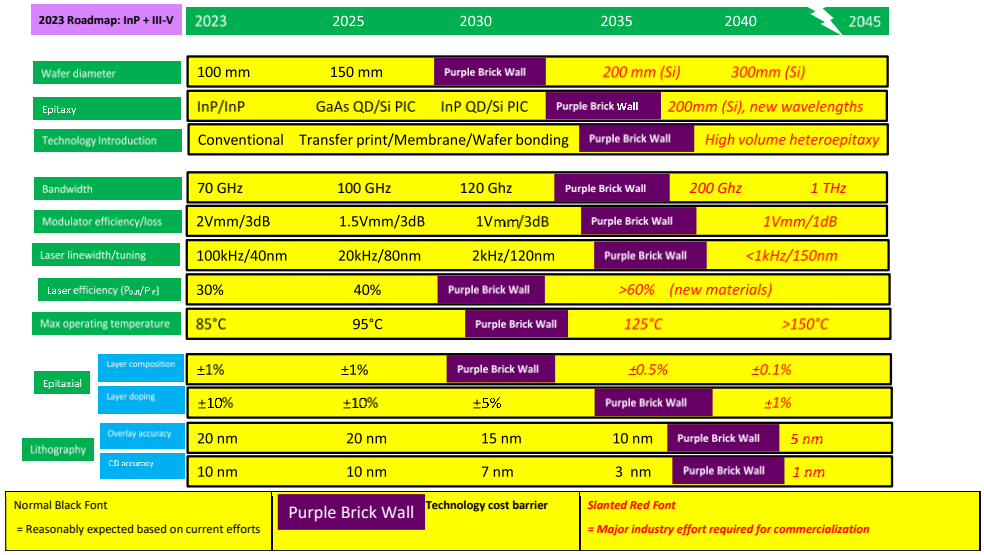

Figure 1: Purple Brick Wall for InP and III-V materials

INTRODUCTION

InP-based PICs have become firmly established in the market place, with suppliers including Lumentum, Finisar, Infinera and Sumitomo deploying large numbers of complex PIC-enabled products today. InP-PIC enabled transceivers already accounted for a 2B€ market in 2022 according to market research by Yole Group and the technology is predicted to expand to >5B€ by 2027. The breakthrough has been made with the roll-out of 100 Gb/s per wavelength link, and the indications are that the InP-PIC market share will continue to increase substantially in applications where device performance is critical.

Discrete devices are produced on 3" and 4" wafers, at volumes of order 10M per month and low complexity PICs comprising of monolithically integrated lasers and modulators are ramping up volume. The current equipment infrastructure is adequate for the cost-performance levels demanded by today's optical communication's market, but the volumes and costs required by emerging applications, especially inter and intra data center interconnects, will put increased pressure on manufacturing equipment and process performance. Furthermore, the requirement to reduce ramp-up time from first design to production calls for increased up-time in production process and predictability.

An important development in this respect is the emergence of "generic" platform technologies, which support development and fabrication of high-performance PICs for a wide range of applications in highly standardized integration processes. The generic approach leads to technology de-risk, a large reduction in the costs of prototyping since it enables sharing the costs of PIC fabrication among many users, and by offering access to a qualified fabrication process which supports volume production. This leads to a substantial lowering of the entry costs for new applicants in the field and opening PICs to new applications and market sectors. Generic open-access foundry service has been pioneered in Europe for InP and silicon photonics since 2007 and is presently experiencing a rapidly increasing interest worldwide. Open access to MPW PIC runs in foundry processes is now offered by a few commercial foundries and several national research centers.

The foundry approach with well-developed processes will have performances that are on par or close to those of highly-customized processes. For specific applications, optimization and customization might be required to allow tuning the offering to achieve ultimate performance. When production volumes are sufficiently large, users of open access foundry processes may decide to customize their foundry process to reach a specific PIC performance improvement. However, by choosing to start product development and validation through a foundry process, the investments in development and qualification will be lower compared to starting from scratch, and will occur at a later stage when the risk in the expected market size is reduced.

The most commonly acknowledged market sectors addressable by PIC technologies are optical transceivers, fiber optic sensors, OCT, BioMEMS and LIDAR. The front-runner market is transceiver technology, which currently receives considerable attention due to a pressing need from internet traffic growth and accelerated data center deployments. Fiber-optic sensing offers a considerable growth opportunity with drivers from the oil industry as well as structural engineering, industrial metrology and aerospace. Compound annual growth rates (CAGR) of order 10% to 20% are observed for photonic solutions in such markets. Medical segments, such as optical coherence tomography (OCT) through to BioMEMs technology, also see considerable growth.

The increased need for free-space mapping and ranging is driving down the costs of solid-state LiDAR technologies, with likely impact in autonomous driving, robotics, vision and virtual reality systems. Although there are commercial implementations already available today, prices are still too high for adoption into large-scale applications. Eye-safety requirements and their potential for advanced beam-forming and signal processing make InP-based PICs an important technology for use in LIDAR systems. As the InP-PIC technology deploys across multiple markets and volumes increase, the corresponding price reduction should enable the use of PIC technologies in larger, more cost-sensitive markets.

SITUATION (INFRASTRUCTURE) ANALYSIS

MATERIALS

The group of III-V semiconductor materials have similar properties to silicon, which is well established in microelectronics. III-V semiconductor materials are epitaxially grown on mono-crystalline semiconductor substrates. The main difference is in the opto-electronic properties, where most III-V semiconductors have a direct bandgap, which is a prerequisite for making efficient lasers and optical amplifiers, a property which silicon is missing. Additionally, several III-V semiconductors, such as GaAs and InP have better electronic properties than silicon, which makes them suited for high-end RF-applications.

The main difference between the various III-V semiconductors is the wavelength range in which they support optical functions like generation, amplification, transmission, and detection of light. For GaAs, which was the first III-V material applied in semiconductor lasers, the operation window ranges from 800-1100 nm, which makes it suitable for short-range communication. GaAs VCSELs are the dominant light source for short distance (< a few hundreds of meters) communications. For InP and its quaternary compounds InGaAsP and InGaAlAs, which can be grown on an InP substrate, the operation window ranges from 1200-1700 nm, which covers the most important wavelengths for high-speed communication over longer distances (O-band, C-band, and L-band). It is, therefore, the material of choice for high-speed communication over long and medium distances.

An additional advantage of InP and its compounds InGaAsP and InGaAlAs is that their optical properties (gain, transparency, absorption and detection, and electro-optic modulation efficiency) can be engineered locally within the wafer while retaining the possibilities for optimizing performance over a wide wavelength range. This makes it the material of choice for use in complex PICs where a wide range of functionalities has to be integrated into a single chip. Examples are coherent transmitters and receivers, and more generally, any circuit where lasers and optical amplifiers need to be integrated with efficient modulators and detectors, as well as low-loss passive-optical elements (e.g., optical filters).

Dielectric materials for passivation and isolation are very similar to those used for silicon microelectronics. Metals for electrical inter-connections are different. Gold is frequently used for III-V semiconductors because of its good electrical and mechanical properties, whereas it is not applied on silicon because of the risk of diffusing into the silicon, where it is very harmful. On the other hand, aluminium and copper are seldom used for III-V materials. In particular copper impurities degrade electrical and optical properties in III-V materials.

Wafers commercially available for III-V materials are smaller than for silicon. For GaAs 4”, 6” and 8” diameters are commercially available. For InP, wafers with 2”, 3”and 4” diameter are commercially available with good quality. Larger 6” wafers are commercially available for R&D purposes, with a slightly larger Etch Pit Density (EPD), which will be improved when the demand increases.

MANUFACTURING PROCESSES

The most important group of processes for the fabrication of III-V photonic components and integrated circuits are:

- epitaxial growth,
- lithography,
- etching of semiconductor material and dielectrics,
- deposition of dielectrics and metals for passivation and metallization,
- grinding and polishing, and
- cleaving and coating.

We will briefly describe them.

Epitaxial growth and regrowth

The first step in the fabrication of most III-V components or integrated circuits is the growth of the epitaxial layer stack, which usually includes a number (up to a few tens) of layers with different compositions and doping types and levels, including Quantum Well or Quantum Dot layers. InP based materials (including the substrate) can be made semi-insulating by doping with Fe atoms, thus enabling efficient electrical isolation of the individual integrated devices and facilitating very-high-frequency operation.

InP-based materials facilitate access to a wide range of bandgaps, which is required to monolithically integrate low-loss passive and high-performance active functions with precise wavelength control and detuning between the laser and its modulator. This requirement increases complexity in epitaxy and material characterization as well as mask design. Several integration technologies have been commercialized (impurity induced layer disordering, butt-joint regrowth and selective area regrowth) each with trade-offs in manufacturing cost, yield and performance. We will briefly discuss the most commonly used approaches for high performance monolithic integration.

In many PICs several different layer stacks are monolithically combined, by using selective butt-joint regrowth: the first grown layer stack is removed everywhere where it is not needed using lithography and etching, after which a second layer with a different layer stack is locally grown. If more than two different layer stacks are needed this process can be repeated. In this way we can get optimal layer stacks for different components (e.g. lasers, modulators, detectors and transparent waveguides) at the regions where those components are needed.

An alternative approach is selective area regrowth (SAG) which is a special integration process relying on local growth rate change induced by proximity to a dielectric mask. In a Quantum Well layer stack this change in the growth rate leads to a shift of the band edge, which can be beyond 100 nm, thus allowing fabrication of lasers, detectors, modulators and transparent waveguide devices with a single growth step.

The quality and control of the epitaxial layer stack is of key importance not only for the performance of active components like lasers and optical amplifiers, but also for modulators and detectors. In this respect III-V technology differs from silicon technology, where epitaxial growth is applied for special cases such as Ge detector layers and SiGe Quantum Wells but is not used in the mainstream technology.

The most frequently used epitaxial growth technique is Metal-Organic Chemical Vapor Deposition (MOCVD), also known as Metal Organic Vapour Phase Epitaxy (MOVPE). For components which require very large dopant gradients, such as Avalanche Photodiodes (APDs), Molecular Beam Epitaxy (MBE) is sometimes used, which operates at a lower temperature. MBE reactors require a high vacuum and are more expensive than MOCVD reactors and have lower deposition rates, which makes them less suitable for very high-volume production. However, they have proven competitive for a number of dedicated applications. MOCVD reactors are provided by a number of manufacturers, with a focus on the large volumes required for fabrication of LEDs. In comparison with the LED market, the PIC market is very small, hindering many manufacturers from making the large investments necessary to develop automated high-performance equipment tailored to PIC manufacturing.

Lithography

The most frequently used lithography is I-line stepper lithography, having a resolution of about 250 nm, though contact lithography may be used for less critical steps. For higher resolution, as required in fabricating gratings, E-beam lithography is typically used, which is a direct-write technique with lower throughput. High resolution tools with high throughput, such as the 193 nm DUV scanners used in microelectronics, are not yet generally available

for InP because the machines were not designed for exposing wafers smaller than 6". It has already been demonstrated that the tools can be adapted for 3" and 4", but they are not commercially available. Optimizations on both the process and the required wafer properties (such as flatness) must be intensified.

Etching

Removing part of the epitaxial layer stack by etching is an important step in any PIC processing. The most frequently used processes are Reactive Ion Etching (RIE) and Inductively Coupled Plasma (ICP) etching. The most frequently used chemistries are CH_4/H_2 and Cl and Br etchants. Etching control and uniformity are usually of the order of a few percent, which is sufficient for many applications, but not for complex high-performance PICs. Edge roughness is extremely important in high-confinement waveguides in order to keep propagation losses low.

The edge roughness is caused by a combination of roughness generating mechanisms in both the lithography and the etching. Etching of dielectric layers is performed with wet chemistry or with RIE or ICP dry etching. If the dielectric layer is used as a hard mask, the etching requirements on edge roughness are very tight. Due to the use of platinum and gold, which are difficult to etch, metal patterns are usually fabricated with lift-off lithography.

Deposition and annealing

Deposition of dielectric layers for passivation or for use as a hard mask (SiO_x or Si_3N_4) is usually done with Plasma Enhanced Chemical Vapor Deposition (PECVD), which can be performed at moderate substrate temperatures. Layer thickness control and uniformity are usually of the order of a few percent, which is sufficient for many applications, but not for all.

For deposition of metals usually electron gun evaporation is used, which has good properties for use as selective deposition in conjunction with lift-off lithography. If better adhesion or better step coverage is required, RF-diode or magnetron sputtering is the preferred alternative.

Usually, an annealing step is required for getting good passivation properties at the interface between the semiconductor and dielectric layer materials and for getting a low resistance at the interface between the semiconductor and contact metals. Here the most frequently used process is Rapid Thermal Annealing.

Cleaving and coating

For singulating PICs from a processed wafer, the most frequently used process is cleaving: small scratches (scribes) are made at the edge of the wafer after which controlled pressure is exercised in order to cleave the wafer along a crystal plane. On proper cleaving, the chip has an atomically flat end facet. For proper cleaving, thinning the wafer down to 100-200 µm is an essential and demanding process, particularly for larger wafer sizes. After thinning the wafer is first cleaved into bars, which contain a series of PICs. After cleaving, the facets are coated to achieve a defined reflectivity; mostly anti-reflection (AR) or high-reflection (HR) coatings are used. This process is performed shortly after cleaving to keep a clean interface. The next step is cleaving or dicing the bars into single PICs. PICs are often tested on bar level.

MANUFACTURING EQUIPMENT

In most cases, InP-fabs use equipment developed to process other materials, such as GaAs and silicon, e.g., equipment for wafer handling, epitaxy (with requirements on control of layer thickness and composition), lithography (high resolution and exposure in the order of 10 units per hour), etching (low-damage, accurate depth control, deep etching) and metrology with 3D measurements and high aspect ratio (HAR) capabilities. However, InP-fabs demand special requirements such as the capability to process smaller wafers (3"and 4") and handling of fragile InP wafers without damage. InP devices have challenging lithography requirements with respect to line-

edge roughness, large depth of focus and extreme critical dimension (CD) control, while additionally the cost of use should match the market size. This requires existing equipment to be adapted to enable the processing of InP.

Currently, most equipment for InP volume manufacturing is partially automated, however, many steps are still performed manually. Full automation will increase process reliability and reproducibility and reduce manufacturing costs. So far the market need has not been large enough to motivate the investments to develop fully automated high-performance equipment tailored for high volumes.

QUALITY/RELIABILITY

InP lasers and GaAs VCSELs produced in large numbers for long, medium and short-range communication links demonstrate that III-V components, if properly manufactured and packaged, show very good reliability with product lifetimes of at least 20 years for telecom parts. For PICs integrating tens of components such as complex tunable lasers, good yields are reported, although no detailed information about yield numbers is provided by the manufacturers. The monolithic encapsulation of active elements within passive circuits does offer a strong yield-driven motivation for tighter integration.

It should be noted that yield is strongly dependent on performance specifications. Yield is influenced by the number of killer defects, but this is usually low. In the same way that silicon electronics is not limited by fundamental density-related yield mechanism, there is no evidence of such a limit for III-V PICs today. Depending on the level of automation and scaling, wafer yield is more likely to be dominated by manual handling, (tight) processing windows, tool stability, and assembly technologies. Experiments with large PICs suggest that with adaption of high-performance manufacturing equipment yields can be high, also for high-performance PICs. Furthermore, it should be noted that yield reductions can occur in several consecutive stages of the device fabrication. For example, assembly and packaging are other manufacturing steps which can introduce significant yield losses.

ENVIRONMENTAL TECHNOLOGY

Material availability

There have been discussions about the availability of InP for a long time. Indium is available in large amounts in ores, but strongly diluted in other materials. It is won as a by-product of other metals (mostly zinc). Prices may increase significantly if the demand increases beyond the level that is supported by the production of other metals. Indium prices showed a strong increase at the beginning of the 20th century (up to $1000/kg) but have since stabilized at roughly half that price. Most indium is used to make indium-tin oxide (ITO), which is an important constituent of touch screens, flat-screen TVs and solar panels. It is also used in microelectronics, and as a special coating for glasses and bearings.

If the demand for PICs increases as expected and we move to 6” wafers which are significantly thicker than 3” wafers, the demand for Indium Phosphide substrates will increase, but this will have a relatively small overall impact. As the bill of materials for PICs is only a small part of the total costs, the effects of an increase in materials costs on the PIC costs are marginal.

Health issues

The use of III-V materials, and in particular InP, has been the subject of health risk analysis. There are indications that InP-based compounds and precursors used in the manufacturing of PICs are toxic on exposure to high concentrations, and in Europe procedures are running to classify InP as toxic material. InP dust can be generated during polishing or thinning of wafers or singulation of PICs, the latter especially when wafers are diced instead of cleaved. Over the years, the PIC and III-V manufacturing industry has implemented stringent safety and health

regulations in their fabrication process, containing dust and other by-products. In an adequate cleanroom environment, the risks for human health are considered to be very low.

TEST, INSPECTION, MEASUREMENT (TIM)

PIC testing contributes significantly to the cost of a module. In Figure 2 the typical stages in the PIC supply chain are presented in the top row, while testing aspects relevant to those stages are shown in the lower row.

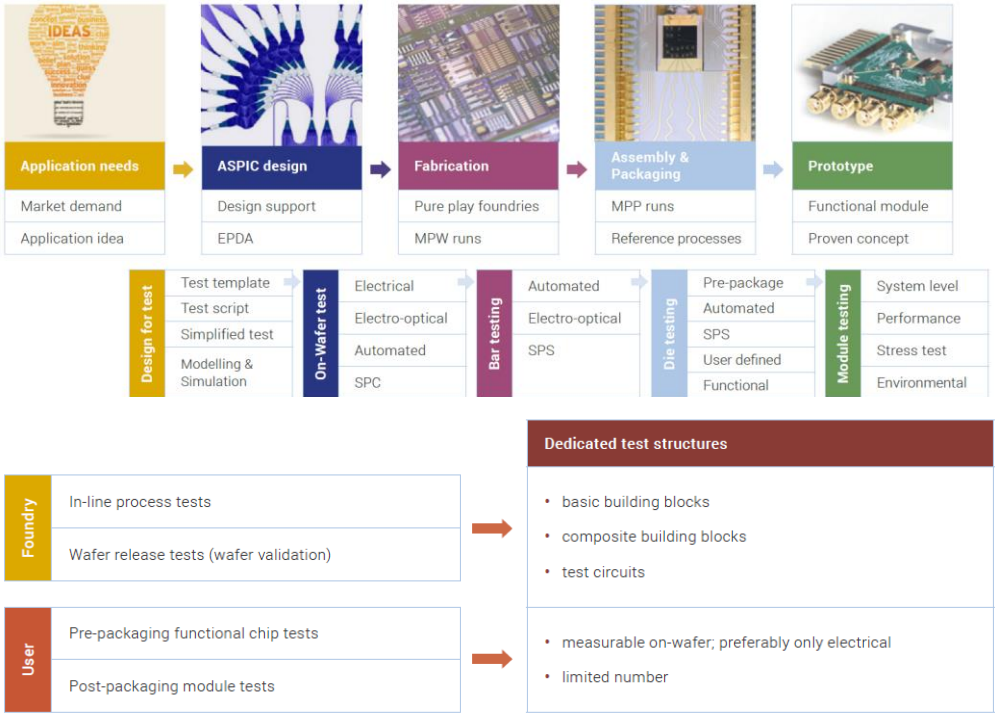

Figure 2: Testing across value/supply chain of Application Specific Photonic Integrated Circuits. (source: JePPIX roadmap 2018)

Significant R&D effort is required to introduce and improve testing at all stages of the PIC process and supply chain. This will allow manufacturers to optimize and accelerate the whole production process and enable early identification of Known-Good-Dies (KGD). In order to facilitate fast testing procedures optical parameters should be measured in an electrical fashion wherever possible. Dedicated test structures relevant for test requirements of foundries and users need to be developed, as depicted in Figure 2.

Smart testing throughout the production process is required to ensure earlier testing to reduce process spread, optimize the PIC manufacturing process windows and maximize yield. An increased level of automation across the full supply chain will result in a reduction of time required for testing and KGD identification. For wafer verification, on-wafer measurements in both the electrical and the optical domain are desirable to allow for testing at various

sites across the wafer prior to cleaving. To this end vertical optical out-coupling structures should be integrated. Viable implementation options could be turning mirrors and grating couplers integrated into appropriate waveguide sections. However, as of today, in contrast to Si based PICs, vertical grating couplers are not routinely used in InP-PICs due to their low coupling efficiency and their large real estate.

MANUFACTURING COST

Scaling laws for InP are similar to other thin film fabrication technologies used in CMOS electronics or silicon photonics. Costs are primarily dominated by the amortization costs for the fab, the complexity of the process (number of process steps) and by the loading of the fab. Material costs usually make up only a small part of the total PIC costs. The cost of InP, silicon photonics (SiPh) or polymer PICs, for example, is not primarily determined by the costs of the material, rather by the cost of the process, which is to a high degree determined by the number and the complexity of the processing steps and by the production volumes.

Figure illustrates the cost dependence of InP PICs on the aggregate annual load of the fab and the size of the wafers run in the fab. It is based on a simple model as described at the end of this sub-section. The load of the fab is expressed in the total number of chips/year for an average chip size of 10 mm^2. For smaller chips the curves will shift to the right, for larger chips to the left.

For volumes much smaller than the fab capacity, the chip cost is dominated by the investments in the fab, which are high for larger fabs. So, for smaller aggregate volumes, large fabs are more expensive than small fabs. For volumes approaching the fab capacity the chip cost is mainly determined by the processing cost, which is only weakly dependent on the wafer size; a large wafer in an expensive fab is not much more expensive than a small wafer in a small fab. This is the main reason that large fabs are more cost effective at high volumes.

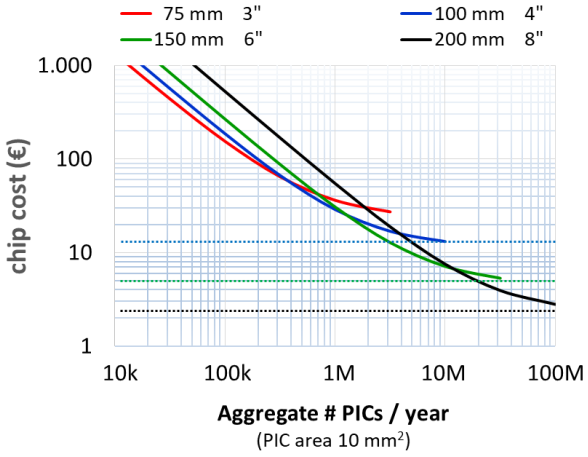

Figure 3. Chip cost as a function of yearly fab load for different fab scenarios, calibrated for an average chip size of 10 mm^2.(source: JePPIX roadmap 2018)

The solid lines indicate the dependence of the PIC costs on the aggregate annual volumes. PIC costs are minimal if the fab is fully loaded. The costs are then dominated by the marginal costs of processing a batch of identical wafers. In a fully loaded fab, smaller volumes using the same process can be fabricated at costs which are close to those of large volumes, as indicated by the horizontal dotted lines.

The line labeled 200 mm is indicative of a small silicon photonics fab. If the PICs are fabricated by a CMOS process in a fab which is fully loaded by electronic ICs, they can be produced at low cost, even when the aggregate volume of photonic ICs is much smaller than the fab capacity, because the aggregate volume is determined by the electronic ICs. For larger wafer sizes of 300 mm operating at higher throughput, the dotted line will be even lower.

If the PICs are fabricated in a dedicated photonic process in a CMOS fab the cost curve will be somewhere between the solid and the dotted curve: the costs of the equipment are shared with electronic IC production, but the costs of the process not. As an example, the propagation losses in a waveguide scale with roughness^2/width^4, and the fabrication tolerances on edge roughness is approximately 10 time greater for SiPh compared with InP; similar scaling apply for phase errors. Further, silicon photonics processes on large wafers typically run on a 45 nm, for which the cost of masks are extremely high. This increases the costs of fabrication of silicon photonics devices significantly at lower volumes.

The graphs are indicative for the dependence of chip cost on aggregate volume and wafer size, but actual costs may differ significantly from the costs shown in the graph. If an old fab, which is already largely depreciated, is used the costs at lower volumes can be significantly lower. Investment costs are also dependent on the wafer capacity of the fab and the degree of automation, which will increase the investment cost and reduce the marginal wafer cost (the horizontal dotted line). Further, yield is an important factor dependent on user requirements: if the requirements are well within the building block specifications and the design rules, it will be high. But if they are close to the process window limits, it can be significantly lower. With these boundary conditions in mind we can draw a few conclusions from the graph:

- Because the square millimeter costs are strongly dependent on the total volume, all users of a fab running an open-access generic process can get their chips at a price corresponding to the aggregate yearly chip volume, even though their own chip volume may be much smaller. This will also make the costs for small users significantly lower.
- For a square millimetre price below 10 €/mm^2, volumes well over 100,000 chips per year are required for a 10mm^2 die area.
- For a square millimetre price below 1 €/mm2, volumes well over 1 million chips per year are required. This cost reduction should be achieved by tool automation.

We anticipate that square millimeter costs of InP PICs will generally remain higher than for SiPh PICs. However, the costs of an (InP) light source and its assembly (or heterogeneous integration) need to be added for SiPh-PICs. Additionally, active InP building blocks such as phase-modulators and lasers can be significantly smaller. When the costs of advanced InP-PICs is reduced to a few Euros/Dollars, InP-PICs are expected to be very competitive for medium or even larger volumes where high performance is required, and also where complex functionalities (a number of lasers and/or optical amplifiers on board) are required.

Explanation of the Model of Figure .
The curves in Figure are based on a very simple model that is useful for a qualitative analysis of the effects of scaling on chip cost. For quantitative purposes it is not accurate enough, although with an appropriate choice of input parameters it can be indicative for cost levels.
The model calculates the cost of a chip from the annual depreciation of the fab cost and the running cost divided by the number of chips that the fab produces per year. And it adds to this the marginal costs of processing a wafer if the fab is (almost) fully loaded. The analysis is done for 4 different fab types with wafer diameters of 3", 4", 6" and 8".

		Fab 1	Fab 2	Fab 3	Fab 4
1	Wafer diameter (mm)	75	100	150	200
2	Fab cost (M€)	75	100	150	300
3	Fab capacity (wafer/yr)	10000	20000	50000	500000
4	Useful wafer area (%)	70%	70%	70%	70%
5	Useful wafer area (mm2)	3,091	5,495	12,364	21,980
6	Reference PIC size (mm2)	10	10	10	10
7	Fab Capacity (PIC/yr)	2.16E+06	8.79E+06	5.56E+07	1.10E+09
8	Depreciation / yr	10%	10%	10%	10%
9	Running cost / yr	4%	4%	4%	4%
10	Yearly Fab Cost (M€)	10.5	14	21	42
11	Marg cost / wafer (k€)	4	4	4	4
12	Yield (%)	70%	80%	90%	100%
13	Profit margin	25%	25%	25%	25%

Row 1 in the table shows the wafer size. The first three fabs could be InP fabs, the latter one a dedicated silicon fab or a fab that processes PICs in a photonic InP membrane on top of an 8" silicon wafer, as described in section 6.1. Row 2 presents the investment in building the fab. It is assumed that fabs for large wafers are more automated and have, therefore, a larger wafer capacity (row 3). Row 4 gives the useful wafer area in % and row 5 in mm^2. Row 6 specifies the average PIC size for which the analysis is done, in this example 10 mm^2. From rows 3-6 the fab capacity in PICs/year (row 7) is calculated. The yearly exploitation cost of the fab (row10) is calculated as the sum of the yearly depreciation (row 8) and the yearly running cost (row 9). Row 11 shows the marginal costs for running a wafer in a fully loaded fab (material and operator cost). The curves in Figure show the yearly fab costs (row 10) divided by the total number of PICs that the fab produces per year, increased by the marginal cost per PIC (row 11 divided by # PICs/wafer), corrected for yield (row 12)

ROADMAP OF QUANTIFIED KEY ATTRIBUTE NEEDS

In this paragraph we describe the present status of the most important building blocks in InP-PICs and the expected evolution of the requirements in 5, 10 and 15 years. The tables are given for PICs operating in the C-band. We consider the addition of similar information for other wavelength bands, such as the O- band and L-band, important but data are not yet available for this edition of the roadmap.

The most important basic building blocks are waveguides, optical amplifiers, electro-refraction and electro-absorption modulators, and detectors.

For the **waveguides,** key properties are propagation loss and minimal bending radius, wavelength and polarization dispersion, which should be very low for polarization independent operation of components based on those waveguides.

For **optical amplifiers**, basic building blocks in any laser, the important parameters are gain and gain bandwidth, output power and efficiency (which is closely related to the transparency current), maximum operating temperature, and polarization properties. The latter property may be of less importance in lasers, which are usually TE polarized.
The most important **modulator** types are electro-refraction (phase) and electro-absorption (amplitude) modulators. **Electro-refraction modulators** are often applied in a Mach-Zehnder configuration. Important properties are electro-optic efficiency, optical loss, linearity and modulation bandwidth. Good modulators have low insertion loss (<1 dB) and high bandwidth (with a traveling wave electrode > 30 GHz). The modulation voltage

is dependent on the length: for low voltages (few Volt) the length is in the order of 1 mm. InP modulators show superior performance in comparison to other technologies.

Electro-absorption modulators are significantly smaller than Mach-Zehnder modulators (size of order 50-100 µm). Due to their small size they can have bandwidths > 50 GHz, but as they operate close to the absorption edge of the semiconductor, they have significantly higher losses than Mach-Zehnder modulators, lower spectral bandwidth, and higher chirp[1] (though zero chirp is possible at certain operating conditions), which makes their commercial deployment in links > 80 km less suitable for high-speed communication in the C and L band.
Detectors show responsivities close to 1 A/W in the C-band, in combination with bandwidths > 40 GHz, and dark currents in the order of 1 nA.

The most important **composite building blocks** are lasers and passive components like MMI-couplers and AWGs. Most platforms support a variety of **lasers**: single-frequency, continuous wave (CW) and short-pulse lasers, tunable and multi-wavelength lasers. Output powers of a few tens of mW are available in most platforms. Laser linewidths are strongly dependent on the laser configuration, ranging from a few MHz to <100 kHz for sophisticated designs. Many laser designs have been reported covering the whole C-band. Energy (wall-plug) efficiencies range to 20% for higher output powers, for low output powers efficiencies are lower. With high-resolution lithography, insertion losses of **MMI couplers and AWGs** can be well below 1 dB (for the central AWG channel).

The tables below address the state-of-the art and future needs for each building block to meet a wide range of applications. The performance metrics are based on current understanding of fundamentally achievable performance of InP building blocks without consideration of a specific application. The ultimate performance achieved by each building block will be largely determined by the integration platform capability in close consideration to application specific requirements and the trade-offs of complexity and performance cost, manufacturability and yield. We emphasize the many device parameters are temperature sensitive; the listed values should be taken primarily for operation at room temperature.

[1] *Chirp is unwanted phase/frequency modulation induced by an intended amplitude modulation*

Basic Building Blocks					
Component property	**2025**	**2030**	**2035**	**2040**	**2045**
1. Waveguide					
Propagation loss / PDL [dB/cm]	0.5-1.0	0.3-0.5	0.3-0.5	0.3-0.5	
Minimum bend radius [□m]	50	25	10	10	
Bend loss per 90 degree [dB]	0.2	0.1	0.01	0.01*	
Wavelength dispersion [(□n/n)/nm]	1×10^{-4}	0.5×10^{-4}	none	none	
Waveguide transparency (<1.5 dB/cm loss) / wavelength range [nm]	1200-1640	1200-1640	1200-1640	1200-1640	
Mode diameter [□m, FWHM]	1.5x1.0	1.5x1.0	0.5 x 0.5*	0.5 x 0.5*	
Back scattering [dB/mm]	-40 dB	<-50 dB	<-50 dB	< -50	
* Transition to high contract waveguide platform					
2. SOA					
SOA Gain [dB]	20	25	30	> 30	
Polarization Dependent gain (PDG) [dB]	2	1	0.5	< 0.5	
Gain bandwidth [nm]	50	100	150	> 150	
Maximum gain ripple [dB]	1	0.5	0.1	0.1	
3-dB gain saturation output power [dBm]	13	16	16	16	
Maximum current density [kA/cm^2]	12	15	15	15	
Operating temperature range [°C]	10…70*	-40…85*	-40…85*	-40…90*	
Noise figure [dB]	6	4	4	4	
SOAs are temperature sensitive; values quoted for room temperature operation. * For operation not at maximum gain; maximum gain typically drops ~2.5 dB/10K					
3. Electro-refraction modulator					
Electro-optic efficiency [V mm]	2	1.5	1	< 1	
Insertion loss [dB]	3	1	1	< 1	
RF 3-dB Bandwidth [GHz]	100	120	200	> 200	
Optical 3-dB Bandwidth [nm]	50	70	100	> 100	
Spurious free dynamic range of second	80	90	>100	> 100	

harmonic distortion SFDR (SHD)[dB x $Hz^{1/2}$]					
Max length [□m]	2000	1000	1000	1000	
Impedance [□]	25-100	25-100	25-100	25-100	
4. Electro-absorption modulator					
Minimum insertion loss [dB]	1	1	1	< 1	
Minimum Extinction ratio [dB]	20	20	20	> 25	
RF 3-dB Bandwidth [GHz]	50	70	100	> 100	
Optical 3-dB Bandwidth [nm]	15	15	15	15	
Max length [□m]	100	100	100	100	
Small Signal Chirp [unity]	1	0	0	0	
Impedance [□]	50	50	variable	variable	
5. Thermo-optic phase modulator					
Power for □ phase shift [mW]	50	20	20	< 20	
Insertion loss [dB]	0.5	0.1	0.1	0.1	
Extinction ratio [dB]	25	25	25	> 25	
Response time [□s]	50	5	5	> 5	
6. Photo detector					
Responsivity [A/W]	>0.9	>0.9	>1	> 1	
Bandwidth (electro-optical) [GHz]	70	100	>100	> 100	
Dark current[nA]	1	1	1	< 1	
3-dB Saturation power [mW]	20	20	20	> 20	
Polarisation dependence [dB]	<1	<1	<1	< 1	
7. Tunable Bragg reflector					
Coupling coefficient [cm^{-1}]	200	200	200	200	
Absolute wavelength control (GHz), during tuning of grating	1	0.5	0.5	0.5	
Coupling coefficient precision [/cm]	±5	±1	±1	±1	
Apodization feature size [nm], Sub-lambda	100	20	20	20	
8. Grating couplers					
Insertion Loss [dB]	2	0.5	< 0.5*	<0.5* * Membrane	

1-dB bandwidth [nm]	30	30	30	30	
Parasitic back reflection [dB]	-20	-30	-40	-40	
9. Polarization rotation section					
Insertion loss [dB]	0.5	0.5	0.5	<0.5	
Optical bandwidth [nm]	50	100	250	250	
Physical length for 90° rotation [µm]	500	100	100	100	
Polarization extinction ratio [dB]	25	30	40	40	
10. Spot size converter					
Input/Output mode diameter ??m]	2-10	2-10	2-10	2-10	
Insertion loss [dB]	0.5	0.3	0.1	< 0.1	
Polarization dependent loss [dB]	0.3	0.1	0.1	<0.1	
Physical length [?m]	300	150	100	< 100	
Parasitic reflectivity [dB]	-30	-40	-50	<-50	
Composite Building Blocks (CBBs)					
1. (Tunable) CW laser					
Output power [mW]	50-70	70-100	>100	> 500	
Tuning range [nm]	45	100	150	150	
Linewidth [kHZ]	100	10	1	< 1	
Relative intensity noise [dB/Hz]	-150	-155	-160	< -160	
SMSR [dB]	>50	>50	>50	> 55	
Operation temperature [°C]	10-75	10-85	10-95	10-110	
2. MMI couplers					
Excess Loss [dB]	0.3	0.2	0.2	< 0.2	
Splitting ratio accuracy [dB]	0.2	0.1	0.1	< 0.1	
Spurious reflectivity [dB]	<-40	<-40	<-40	<-40	
Optical bandwidth [nm]	60	80	100	>100	
3. MMI reflectors					
Insertion loss [dB]	0.5	0.3	0.2	< 0.2	
Reflection/transmission ratio accuracy [%]	5	3	1	> 1	
Optical bandwidth [nm]	60	80	100	100	
4. AWG (de)multiplexers					

Excess loss [dB]	3	2	1	< 1	
Maximum number of channels	20	30	40	> 40	
Minimum channel spacing [GHz]	100	50	50	> 50	
Excess loss for outer channels [dB]	2	1	0.5	0.5	
Crosstalk [dB]	-30	-35	-40	> -40	
5. Polarisation splitter/coupler					
Insertion Loss [dB]	1	0.5	< 0.5	< 0.5	
Rejection unwanted polarisation [dB]	>20	30	> 30	> 30	
6. RF interconnection					
3 dB frequency at 2 mm length [GHz]	70	80	>100	> 100	
Propagation loss at maximum frequency [dB/mm]	0.3	0.3	0.3	< 0.3	
7. Mach-Zehnder modulator					
Electro-optic efficiency [V mm]	2	1	<1	< 1	
Insertion loss [dB]	5	3	1	< 1	
RF 3-dB Bandwidth [GHz]	70	100	>100	> 100	
Electrical return loss [dB]	<-10 dB	<-15 dB	<-20 dB	< -25 dB	

CRITICAL (INFRASTRUCTURE) ISSUES

For manufacturing equipment special attention is required in the following fields:

WAFER HANDLING

Due to the fragile nature of InP, robotic wafer handling is required throughout the production line to reduce instances of breaking and accumulation of particles. To meet yield expectations in high performance PICs, InP PIC production equipment should support cassette-to-cassette loading.

LAYER THICKNESS AND ETCH DEPTH CONTROL AND UNIFORMITY

Optical waveguide properties are very sensitive to waveguide dimensions, requiring well defined process windows delivering dimensional control down to the nm level. As an example, a 1-nm variation in the width or height of high-contrast waveguides leads to 100 GHz wavelength shift in wavelength selective devices, which means that nm-scale variations in waveguide dimensions over the wafer can have a significant effect on the component properties. Enhanced in-situ measurement capabilities are needed to control the layer growth in epitaxy and PECVD and the etch depth in the etching tools. This will enable systematic process control and optimization across wafer topologies. In-line particle detection capabilities are expected to accelerate process control to improve fabrication yields.

TOOL-STATUS CONTROL

Accurate production tool status control and compensation, including self-cleaning methods are important for increased throughput and process uniformity. Self-cleaning will be required for epitaxial equipment, and increased reproducibility in terms of layer thickness and materials composition with control down to ± 1 % in the coming years and an order of magnitude better on the longer term (see tables on technology needs).

LITHOGRAPHY

It is important that the resolution and reproducibility of 193 nm DUV lithography becomes available also for wafer diameters below 200 mm, including 4" and 6". Because of its small depth of focus, high resolution optical lithography has increased requirements on wafer flatness, and there is an insufficient number of suppliers meeting the specifications for precision lithography.

TESTING

Testing of process parameters (geometrical, optical and electrical) should become available as early in the fabrication as possible. Automatic testing of dedicated test structures should be performed at wafer level. New inspection methods and analytics are needed to correlate in-line test, off-line product test and product release test in a generic, application independent way.

PACKAGING AND ASSEMBLY

Efficient and compact Spot-Size converter arrays and etched angled facets are important for low-loss low-reflection coupling to fibre arrays and multi-port interposers. For ease of coupling and assembly the angled facets should be positioned such that the output beams leave the chip normal to the chip edge. For efficient coupling to RF-electronics, RF-waveguides should be integrated in the PIC design.

TECHNOLOGY NEEDS

By improving on manufacturing accuracy, fidelity and reducing attainable feature sizes and tolerances, more sophisticated and more precise designs can be made on component level, leading to steady advancements of the performance metrics. Accurate epitaxy and precision lithography can lead to more capable functional actives and lower losses for passive components. Higher resolution and smaller feature sizes translate to compact components that are more energy efficient and operate at higher speeds. In this section we describe the requirements on the manufacturing technology that are necessary to realize the component performance targets listed in the section 'Roadmap of Quantified Key Attribute Needs' in a cost-effective high-volume process.

SUBSTRATES

Today, good quality 3" and 4" InP-substrates are commercially available from several manufacturers. Wafer flatness is sufficient for stepper lithography requirements. However, for high-resolution DUV lithography wafer flatness must be improved. To allow for accurate cleaving of the final chips, the output waveguides should be aligned to a crystal plane. For this, the wafer flat has to be oriented along the crystal plane which can be offered by most substrate manufacturers.

INCREASE OF PRODUCTION CAPACITY

For the expected growth of the PIC market it will be necessary to increase the wafer capacity of existing and new fabs. This can be done by increasing the size of the wafers or by further automation of the process using robots for loading and unloading machines, or by a combination of both. Semi-Insulating InP-wafers of 6" are presently available, albeit with slightly larger Etch-Pit Density (EPD). However, with increased demand the quality of 6" wafers will be improved to match the quality of today's smaller wafers.

An alternative way to reach higher wafer capacity is a fully automated fab working with 4" wafers. It is not yet clear which way is the most cost effective one. A further increase to 8" wafer diameter will require a different approach in order to avoid extremely thick substrates. Here technologies for bonding InP membranes or more complex layer stacks on silicon offer an alternative route. It would still require smaller InP wafers for growing the epitaxial layer stack, but the subsequent processing could then be done on 8" or even larger wafers. The wafer bonding technique is mastered at R&D level and efforts are made to make this technology more broadly available.

InP Substrates	[unit]	2025	2030	20035	2040
Wafer diameter	mm	150	150	200[2*]	> 200 [2] *Epi reactor development necessary
Total Thickness Variation	□m	1	0.5	0.5	< 0. 5
Etch Pit Density of S.I InP:Fe	cm^{-2}	$< 5.10^3$	$< 1.10^3$	$< 1.10^3$	$< 1.10^3$
Minimum resistivity SI	□cm	$>10^7$	$>10^7$	$>10^7$	$> 10^7$
Flat orientation	degrees	±0.01	±0.01	±0.01	±0.01

[2] 200 mm wafers assume that the InP wafer stack is bonded on a silicon substrate

EPITAXY

For commercial epitaxy reactors layer thickness and composition reproducibility are in the order of a few percent. In the coming decade this should be improved by an order of magnitude to improve the yields for highly demanding components. Further, it is important to reduce the number of defects, especially in regrowth steps.

This will require in-situ cleaning procedures both for the reactor chamber and for the wafer surface in combination with in situ monitoring of particles and their distribution on the wafer. For improving operational reproducibility, automatic loading and unloading of reactors is of key importance. Parallel to the increase in performance, operational techniques will have to be developed for measuring any improved performance and optimize processes and methods.

(Epitaxial) growth/layer deposition	[unit]	5 years	5-10 years	10-15 years	Comments
layer thickness uniformity	%	± 1	± 0.2	± 0.1	Over the whole wafer, with edge exclusion TBD, assuming wafer size below, large scale reactor
layer thickness reproducibility	%	± 1	± 0.2	± 0.1	From run to run
layer composition uniformity	PL (nm)	± 1 nm	± 0.5	± 0.1	With wafer exclusion at wafer edge
layer composition reproducibility	PL (nm)	± 1 nm	± 0.5	± 0.2	From run to run
doping concentration uniformity	%	± 10	± 5	± 1	Over the whole wafer, exclusion edge
doping concentration reproducibility	%	± 5	± 5	± 1	From run to run
Other dopant materials	name	C, Be, Mg			Alternate stable/abrupt p-dopant precursor
Defect/particle density	cm^{-2}	5	2	1	Depends on particle size < 1-20 microns; for one growth run
Wafer diameter	mm	150	150	200	
# wafers per run					Market driven and depends on reactor development

DEPOSITION AND ETCHING

The most important properties of deposition and etch equipment are the reproducibility and uniformity of layer thickness and etch depth. Waveguide properties like propagation constant and polarization dispersion are extremely sensitive to width and thickness variations, down to the nm-level. In order to approach that, reproducibility and uniformity will have to be improved by an order of magnitude in the coming decade, from a few percent today to one or a few tenths of a percent in ten years. In situ monitoring of layer thickness, etch depth and tool status will be necessary to achieve such performance. Just like for epitaxy reactors, automatic (robot) loading and unloading is crucial for reproducible operation.

Dry etching	[unit]	5 years	5-10 years	10-15 years	Comments
side wall roughness (rms)	nm	5	2	1	< 2 microns
side wall angle accuracy	degree	± 1	± 0.5	± 0.2	
etch depth uniformity	%	± 1	± 0.5	± 0.1	Over the whole wafer with edge exclusion
etch depth reproducibility	%	± 1	± 0.5	± 0.1	From run to run
Maximum etch rate	□m/min	5	10	10	Chemistry dependent
CD* Loss	nm	10	3	1	
CD* uniformity	nm	5	3	1	Over the whole wafer with edge exclusion
CD* reproducibility	nm	10	3	1	From run to run
Smallest slot width	nm	100	50	20	Over the whole wafer; will be aspect ratio dependent
Smallest line width	nm	100	50	20	Over the whole wafer; may differ for dense and isolated lines
Minimum grating pitch	nm	200	180	180	Over the whole wafer

* Critical Dimension

Deposition of dielectrics	[unit]	5 years	5-10 years	10-15 years	Comments
Layer thickness uniformity	%	± 1	± 0.5	± 0.2	Over the whole wafer
Layer thickness reproducibility	%	± 1	± 0.5	± 0.2	From run to run

Metal deposition	[unit]	5 years	5-10 years	10-15 years	Comments
Temperature budget	[K]	<350	<350	<350	Compatible with lift-off patterning
Layer thickness Uniformity	%	2	1	1	
Layer thickness reproducibility	%	± 2	± 1	± 1	From run to run

LITHOGRAPHY

For good lithography performance and to avoid damage during exposure it is important to remove contact lithography from the process flow and replace it by projection lithography. Today resolutions up to 250 nm can

be achieved with stepper lithography. For non-flat surfaces (e.g. after several epitaxial overgrowth steps) and higher resolutions, e.g. in gratings, E-beam lithography is used. Because this is a direct-write technology, it is difficult to scale it to very high throughput without installing a large number of machines. Consequently, optical lithography is a better option provided that processing allows for a sufficiently flat surface morphology. For the realization of the resolution required for gratings 193 nm DUV lithography provides an important solution. This resolution is available in scanner lithography machines. However, today these machines cannot handle wafers smaller than 6". ASML has adapted one machine for handling 3" and 4" which is presently installed at the Nanolab cleanroom at TU Eindhoven. On this machine high quality gratings and low-loss AWGs with very narrow (100 nm) inter-waveguide gaps have been demonstrated. An additional advantage of DUV scanners is the process control and reproducibility, which is significantly better than for E-beam lithography. However, these machines are not yet commercially available. For high-performance high-volume manufacturing of PICs it is of utmost importance that such technologies become available in InP PIC process lines.

Stepper/scanner Lithography	[unit]	5 years	5-10 years	10-15 years	Comments
Overlay accuracy	nm	20	10	5	
Resolution	nm	100	50	20	Needs technology development
Required Wafer Flatness	m ttv[3]	1	1	1	
Required Wafer Flatness	m ttv	0.5	0.2	0.2	
CD Loss	nm	10	3	1	
CD uniformity	nm	10	3	1	
CD reproducibility	nm	10	3	1	
Resist thickness	nm	100	100	100	
Smallest slot width	nm	100	50	20	
Minimum grating pitch	nm	200	180	180	

E-Beam Lithography	[unit]	5 years	5-10 years	10-15 years	Comments
Overlay accuracy	nm	10	5	2	
Speed	wafers/hr	2	5	10	One response requiring 200/hr
Resolution	nm	10	10	5	
Required Flatness requirements	µm	5	5	5	
CD Loss	nm	10	3	1	
CD uniformity	nm	10	3	1	
CD reproducibility	nm	10	3	1	
Smallest slot width	nm	100	50	20	
Minimum grating pitch	nm	200	180	180	

OTHER PROCESSING STEPS

[3] ttv: total thickness variation

The impact of and interaction between annealing, planarization, passivation and other steps during wafer fabrication must be carefully considered to achieve high performance, high stability and high yield devices/PICs. Thermal annealing processes usually occur after dielectric deposition steps (e.g., to adjust film stress, hydrogen content), metal deposition (to promote adhesion and contact formation to semiconductor layers), and in some planarization and reflow processes. The optimum thermal budget (temperature and time) for each step will depend on the materials and fabrication sequence, but some values are indicated in the table below. Contact resistance is routinely measured using standard PCMs but the effect of annealing dielectric and metal film stacks on other device properties can be more difficult to measure. Several steps including annealing (Ohmic contacts, dielectric and implant activation) will need to be automated to batch processes to reduce cycle time.

Exposed III-V surfaces are well-known to have poor stability of their chemical, electronic and optical properties, unlike silicon where the fabrication of extremely high-quality stable oxide – Si interfaces are reproducibly obtained. For example, exposed junctions during fabrication of lasers, modulators, detectors and other waveguides (by etching, diffusion or cleaving) will require a passivation coating which needs to remain stable (low leakage) through all remaining (thermal) steps in fabrication, packaging and reliability tests, and eventually at all operating conditions. The pre-cleaning and deposition of the passivation layer should not degrade the target surface roughness or optical loss of etched waveguides.

Integration of the basic building blocks into functioning PICs involves tapered etching or etching and regrowth as part of waveguide formation. In addition to sidewall passivation, the reflections from interfaces between different parts of the PIC waveguide need to be controlled to achieve the required insertion loss and extinction ratio in modulators, for example. OTDR measurements on singulated devices or bars are used to assess the contributions from these interfaces, but some form of on-wafer assessment using etched facets or surface grating couplers may provide a useful PCM for manufacturing control.

Annealing	**[unit]**	**5 years**	**5-10 years**	**10-15 years**	**Comments**
Ohmic Contact formation (RTA)	[K/s]	650-700/ 20 - 200	TBD	TBD	Materials and device dependent
Dielectrics (PECVD)	[K]	725	TBD	TBD	Post deposition adjustment of H content and stress
Wafer level burn-in/screening	[K]	~450	TBD	TBD	Develop methods for PICs
Planarization	**[unit]**	**5 years**	**5-10 years**	**10-15 years**	**Comments**
BCB (cure)	[K,hour]	500/10			Coat & cure processes adjusted for topography
Required flatness	nm	500	200	100	Will depend on etched topography across the wafer.and planarizing materials used Impacts litho CD control/uniformity

Passivation	[unit]	5 years	5-10 years	10-15 years	Comments
Deposition Temperature	[K]				
Junctions and facets (PECVD)	[K]	575	TBD	TBD	Low damage conformal processes. ALD?
Final passivation (PECVD nitride)	[K]	575	TBD		For non-hermetic packaging. Other materials?
MOCVD (selective) regrowth	[K]	850 - 900			For spot size convertors, blocking layers and waveguides

Singulation	[unit]	5 years	5-10 years	10-15 years	Comments
Facet definition		cleaving	etching		
Die singulation		cleaving	dicing		
Facet position accuracy	[µm]	5	0.5	0.05*	*Etched facet position limited by stepper overlay and etch profile control

PRIORITIZED RESEARCH NEEDS (> 5 YEARS RESULT)

As a major research priority, we consider the integration of photonics and electronics. The drive for higher performance and lower cost will require close integration of driver and control electronics with photonics. To reduce the cost of integration it has to be done at a wafer scale, either by hybrid or by heterogeneous integration. Understanding the performance requirements at the system level will drive the optimization of the integration platform and process (mechanical, thermal, reliability, etc.). This may likely need a holistic development approach or optimization, considering the performance requirements from the integrated system.

PRIORITIZED DEVELOPMENT & IMPLEMENTATION NEEDS (< 5 YEARS RESULT)

1. Epitaxy defect/particle density < 10 cm^{-2}. Fully automated epitaxial growth equipment
2. Dry etching - etch depth control <1% <20nm
3. Passivation reliability for non-hermetic packaging
4. E-beam mask overlay accuracy 10 nm
5. InP substrates TTV < 1 µm for scanners
6. Lithography resist selectivity (resist/etch, wafer TTV < 1 µm)
7. Etched angled facets for low-reflection coupling from and to beams normal to the chip edge (important for easy coupling to fibre arrays)

GAPS AND SHOWSTOPPERS

Crucial for the development of InP-based technology into high-volume technology with high yields is the development of improved equipment, as described in the sections 'Critical (Infrastructure) Issues' and 'Technology needs'.

RECOMMENDATIONS ON POTENTIAL ALTERNATIVE TECHNOLOGIES

As a promising but also challenging technology for moving towards larger wafer sizes we consider technologies for processing InP-based wafer stacks on silicon substrates. This requires bonding of unprocessed or partially processed InP wafers stacks on silicon or CMOS wafers, and removing the InP substrate. Integration on CMOS will require the epitaxy to be performed before bonding and develop a process flow compatible with CMOS line.

CONTRIBUTORS